DESIGN AND PERFORMANCE ANALYSIS OF FINFET BASED DIGITAL CIRCUITS

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A Thesis Submitted to the Academic Faculty in Partial Fulfillment of the Requirements for the Degree of

BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

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Gazipur, Bangladesh

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Date: 3/10/25

Declaration

We, the undersigned, hereby declare that the work presented in this thesis entitled **Design and Performance Analysis of FinFET Based Digital Circuits** is the result of our own effort and investigation, carried out under the supervision of **Dr. Md. Masum Billah**, Assistant Professor, Department of Electrical and Electronic Engineering, Islamic University of Technology (IUT), Gazipur, Bangladesh.

To the best of our knowledge and belief, this work has not been submitted, either in whole or in part, for the award of any degree or diploma at any other university or institution. All sources of information used in this thesis have been duly acknowledged.

Title of the Thesis: Design and Performance Analysis of FinFET Based Digital Circuits

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List of Acronyms

Acronym	Elaboration
CMOS	Complementary Metal-Oxide-Semiconductor
FinFET	Fin Field-Effect Transistor
CNFET	Carbon Nanotube Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SOI	Silicon-On-Insulator
TCAD	Technology Computer-Aided Design
PTM	Predictive Technology Model
PDP	Power Delay Product
DIBL	Drain-Induced Barrier Lowering
SS	Subthreshold Slope
LECTOR	Leakage Control Transistor
INDEP	Input Dependent Control
VDD	Drain Supply Voltage
IDS	Drain-to-Source Current
VGS	Gate-to-Source Voltage
Vth	Threshold Voltage
SRH	Shockley-Read-Hall Recombination
BGN	Band Gap Narrowing
FLDMOB	Field Dependent Mobility
BQP	Bohm Quantum Potential
VS-CNFET	Virtual Source Carbon Nanotube Field-Effect Transistor
PUN	Pull-Up Network
PDN	Pull-Down Network
OBE	Outcome Based Education
CO	Course Outcome
PO	Program Outcome
RCA	Ripple Carry Adder
LCT	Leakage Control Transistor
PVT	Process, Voltage, Temperature

HSPICE	Hierarchical Simulation Program with Integrated Circuit Emphasis
EDA	Electronic Design Automation
ITRS	International Technology Roadmap for Semiconductors
ADC	Analog-to-Digital Converter
PSRR	Power Supply Rejection Ratio
LFSR	Linear Feedback Shift Register
VLSI	Very Large Scale Integration
CNT	Carbon Nanotube
NCNTFET	Negative Capacitance CNTFET
GNRFET	Graphene Nanoribbon Field-Effect Transistor

Acknowledgements

First and foremost, we express our heartfelt gratitude to the Almighty Allah for His infinite blessings, guidance, and mercy, which have enabled us to complete this thesis successfully. Without His grace, this work would not have been possible.

We would like to extend our sincere gratitude to the University of Arizona for providing the Predictive Technology Models (PTM) used for CMOS and FinFET simulations, which served as a vital foundation for our research. We also express our deepest appreciation to Stanford University and the Massachusetts Institute of Technology (MIT) for developing and sharing the Stanford–MIT Virtual Source CNFET model, which enabled the accurate simulation and analysis of CNFET-based circuits. Their open-source contributions have been instrumental in advancing academic research and innovation in nanoscale device technologies.

We are profoundly grateful to our respected supervisor, Dr. Md. Masum Billah, Assistant Professor, Department of Electrical and Electronic Engineering, for his continuous guidance, valuable insights, and unwavering support throughout the completion of this thesis. His expert supervision, patience, and motivation have been pivotal to the success of our research work.

Finally, we would like to convey our sincere thanks to the Department of Electrical and Electronic Engineering, Islamic University of Technology (IUT), for providing the necessary facilities, resources, and academic environment that made this research possible.

Abstract

The continual downscaling of transistor dimensions in advanced semiconductor technologies has accentuated the limitations of conventional planar CMOS devices, notably the pronounced short-channel effects: threshold voltage roll-off and elevated leakage currents observed at deep nanometer regimes. To address these constraints, this study presents a comprehensive *Design and Performance Analysis of FinFET-Based Digital Circuits*, focusing on *Inverter, NAND* and *NOR* gates implemented using predictive SPICE models. FinFET technology, with its tri-gate structure and superior electrostatic control, is evaluated alongside conventional CMOS and emerging CNFET architectures to assess improvements in speed, leakage, and energy efficiency.

Device-level simulations were conducted in Silvaco TCAD to validate a *20 nm FinFET structure*, while circuit-level analyses employed Cadence Virtuoso using PTM 32 nm CMOS, PTM 7 nm FinFET, and Stanford–MIT VS-CNFET models. Key performance metrics - *propagation delay, static leakage power, average power*, and *power-delay product (PDP)* - were extracted for cross-technology comparison: results showing FinFET circuits to achieve over ***95% reduction in static leakage*** and nearly ***90% improvement in PDP*** relative to CMOS, owing to enhanced gate control and reduced parasitics. CNFET circuits exhibit the best theoretical performance with ultra-low leakage and minimal PDP, attributed to quasi-ballistic carrier transport.

To further optimize power consumption, two circuit-level leakage control schemes, **LECTOR** and **INDEP**, were implemented. The *LECTOR–FinFET* configuration achieved consistent leakage suppression with minimal delay penalty, whereas *INDEP–FinFET* offered more aggressive leakage reduction - up to ***92%*** - at the cost of higher propagation delay and PDP.

Overall, ***FinFET integrated with LECTOR*** optimization demonstrates the most practical and energy-efficient architecture for nanoscale digital circuit design, whereas CNFET remains a promising candidate for future ultra-low-power VLSI systems pending fabrication maturity.

Keywords:

FinFET, CNFET, CMOS, Leakage Reduction, LECTOR, INDEP, Power Delay Product (PDP), Short Channel Effects(SCE), TCAD Simulation, SPICE Modeling, Low Power VLSI Design, Nanoscale Devices.

Literature Review

1. ***Performance analysis for reliable nanoscaled FinFET logic circuits***	
Authors	Umayia Mushtaq • Vijay Kumar Sharma
Year	2021
Summary	* They designed FinFET logic circuits and implemented INDEP and LECTOR techniques to reduce the leakage current. * Leakage power Dissipation Saved: 94.91% for INDEP and 74.65% for LECTOR (compared against MOSFET circuits) * The final conclusion is that INDEP is the better technique to reduce the leakage current. * Performed Reliability Analysis using Monte Carlo Simulations on Ring Oscillator circuit for INDEP
Points of comparison	*Leakage power dissipation, *Propagation Delay, *PDP
Software	ELDO Simulator
Node	16nm (Model: MG BSIM4 PTM)
Circuits	Inverter, NAND-2, NOR-2
Limitations	*Ignores ON-State current, *Does not discuss thermal Performance, *Works with basic Logic styles only

2. ***Design of Three Stage Dynamic Comparator with Tail Transistor using 20nm FinFET Technology for ADCs***	
Authors	Monalisa Chatterjee , Ravish Gupta
Year	2022
Summary	*They simulated two configurations of 3-Stage Comparator circuits, one with tail transistor and another without. Both designed with 20 nm FinFET technology. *The two configurations were compared against each other. The Config. with the Tail Transistor performed better (20% less Power Usage, 17% Overall Efficiency) with some drawbacks (2.4-14% larger delay)
Points of comparison	* Energy Efficiency, * Delay
Software	Cadence Virtuoso
Node	20nm
Circuits	3 stage Comparator Circuit with and without Tail Transistor
Limitations	* Comparison with MOSFET circuits missing * Misses out on different logic styles

3. ***FinFET-Based High-Frequency and Low-Power Voltage-Controlled Astable Multivibrator***	
Authors	Amir Baghi Rahin, Afshin Kadivarian , Morteza Dadgar , Vahid Baghi Rahin

Year	2024 (Conference Paper)
Summary	*Astable Multivibrator circuits were designed using FinFETs and their performance was simulated. *Observations made while varying: 1. Power Supply Voltage (Vdd), 2. R and C values, 3. Control Voltage (Vc) *Comparisons made against Other technologies such as CMOS, CNTFET, NCNTFET,PCNTFET and FinFET of 45nm Node.
Points of comparison	* Frequency, *Power Dissipation, *Sq. Wave Amplitude, *Rise and fall time, *Slew rate, *Fr. Tuning Ability *Power consumption
Software	Synopsys HSpice
Node	32nm
Circuits	FinFET based Astable Multivibrator
Limitations	* Older Technology Nodes

4. ***Design and Analysis of Heterojunction Inverted-T P-FinFET on 14nm Technology Node for Use in Low-Power Digital Circuits***	
Authors	Shekhar Verma · Suman Lata Tripathi
Year	2023
Summary	*They've used the Cogenda TCAD tool to design inverted and T-shaped-Fin P-FinFET and N-FinFET devices. Adjustments made using the PTM-MG Models and published data. *They evaluated On State current, Off state current, On to Off current ratio, DIBL, Subthreshold Slope for the devices. *Process Variation was introduced in terms of Work Function, Mole Fraction, Si-Ge material and temperature. *They constructed an inverter with this FinFET design and then compared its Noise margin, Average delay and Average power with conventional CMOS inverters.
Points of comparison	*On State current, *Off state current, *On to Off current ratio, *DIBL, *Subthreshold Slope, *Average Delay, *Average Power
Software	Cogenda TCAD
Node	14nm (PTM-MG ITRS roadmap 2015)
Circuits	Inverter
Limitations	* Works with only basic Inverter circuit, *misses out on other Logic Styles

5. ***Design and Analysis of High Performance FinFET-Based Linear Feedback Shift Register for Cryptography Applications***	
Authors	M. Susaritha1 * and J. Senthilkumar
Year	2024
Summary	*They simulated LFSR circuits with 2-fin and 3-fin FETs and compared them against Planar MOS circuit, they also analyzed the effect of Process Variation *3 fin design consumes lowest power

	*FinFET LFSR shows 8% power reduction compared with CMOS LFSR and also provides faster switch performance and higher density
Points of comparison	*Ion, *Ioff, *Pd,*C, *Id, *Vd
Software	Microwind
Node	Didn't mention
Circuits	*D Flip-Flops, *XOR Gate, *LFSR
Limitations	The work focuses on simulated FinFET-based LFSR performance and does not examine hardware implementation, power–security trade-offs, or scalability in practical cryptographic systems.

6. ***Design and Simulation of SF-FinFET and SD-FinFET and Their Performance in Analog, RF and Digital Applications.***	
Authors	Syed Samsuz Zaman, Pankaj Kumar, Manash Pratim Sarma, Ashok Ray and Gaurav Trivedi
Year	2017
Summary	* TCAD simulation of Triple gate Step Fin FinFET (SF-FinEFT) and Step Drain FinFET(SDFinFET) field effect transistor * Fringing electric field problem can be reduced by using gate stack structure using silicon dioxide between channel and high-k dielectric region. *Strained silicon increases mobility of carriers, modifies the current transport properties, increases the drive current. *Gate length to fin width ratio should be high for low DIBL and high Ion to Ioff ratio.
Points of comparison	*Ion, *Ioff, *Ion-Ioff ratio, *SS, *DIBL, *transconductance, *drain conductance, *trans-conductance generation factor, *total gate capacitance, *cut-off frequency, *gain frequency product, *noise margin and *propagation delay.
Software	TCAD
Node	Didn't mention.
Limitations	The study omits process variation, parasitic, and thermal effects that could alter real-world SF- and SD-FinFET performance.

7. ***D-Latch modules designed using 18nm FinFET Technology***	
Authors	G. Yamini, T. Vinitha, S. Sanath Reddy
Year	2020
Summary	They said there are two types of FinFET. Shortedgate FinFET and Independent-gate FinFET. FinFET having thick oxide on the top of the fin is called Double gate FinFET. FinFET having thin oxide on the top of the fin and the sides is called as Tri-gate FinFET. The fringe capacitances will be reduced by using the Tri-gate FET's. They implemented 4 designs to get the result of D latch. They used existing models to compare like GNRFET.
Points of comparison	lower leakage current and lower power consumption. FinFET consumes less power and has low power delay product when compared to traditional D-Latch designs.

	LVT AND HVT--- Power and Delay comparison.
Software	Cadence virtuoso tool
Node	18nm
Circuits	A power supply of 1V at a frequency of 1GHz. LVT and HVT FinFETs (For calculating power and delay calculations)
Limitations	Cadence software allows only two levels to simulate. So they couldn't simulate more than that.

8. ***PERFORMANCE ANALYSIS OF FINFET BASED INVERTER, NAND AND NOR CIRCUITS AT 10 NM ,7 NM AND 5 NM NODE TECHNOLOGIES.***	
Authors	A. Lazzaz, K. Bousbahi, and M. Ghamnia
Year	2023
Summary	This paper presents a comparative study of CMOS gates designed with FinFET 10 nm, 7 nm and 5 nm technology nodes. Electrical parameters like the maximum switching current ION, the leakage current IOFF, and the performance ratio ION/IOFF for N and P FinFET with different nodes are presented in this simulation.
Points of comparison	Leakage current Parasitic junction and drain/source capacitance Ls, Ld, Lg, Tox, Hfin, Wfin
Software	Microwind 3.8 software
Node	10, 7, 5 nm FinFET
Circuits	- NOT GATE- NAND GATE- NOR GATE
Limitations	The work is restricted to simulated results for selected logic gates and does not include fabrication-level validation or performance under varying environmental conditions.

9. ***Design of FinFET Based Op-Amp Using High-K Device 22 nm Technology.***	
Authors	Vasudeva Ga1, Mandar JATKARa , Tripti R KULKARNIa , Roopa R KULKARNia , Bharathi GURURAJb and Tejas M Pa
Year	2023
Summary	Implement Opamp utilizing the model characteristics of FinFet using high k gain in the context of 22 nm technological advancements. Used SAR as the Analog to digital converter because of its significant advantages in terms of power dissipation , shortened conversion time by removing the clock from the SAR logic, the improvement in conversion time remains limited. have presented high-resolution ADCs operating at 150 MS/s with low power dissipation. They have evaluated development of high-resolution, high-speed, and low-power ADCs using SAR logic in the context of 22 nm technology.
Points of comparison	Channel Width, Oxide level I, Oxide level II, Gate length, Source/drain length extension, Gate Source/gate overlapping. Comparison with 32nm: PS_RR- 28% improved, UGB 99.99%, Slew rate 96.2%.
Software	1.ELDO simulator (phase margin and gain simulations) 2. HSPICE simulator

Node	22nm
Circuits	SAR, Difference Amplifier
Limitations	The Power Supply Rejection Ratio (PSRR) is expected to be approximately 45 dB, and it shouldn't go above 45 dB. About 52 dB are measured by the PSRR that was attained.

10. ***Energy-Efficient Design for Logic Circuits Using a Leakage Control Configuration in FinFET Technology.***	
Authors	Shams Ul Haq · Vijay Kumar Sharma
Year	8 March 2024
Summary	Proposes a leakage power control technique based on the reverse body bias effect. The transistor configuration has been proposed to put a curb on the leakage power. The results have been approved on some fundamental logic gates and a C17 ((ISCAS-85) benchmark circuit. The power optimization and PDP optimization of 45.47% and 49.12% have been observed in the low-power NAND gate. The proposed 2-input NOR gate depicts a leakage power and PDP mitigation by 69.60% and 70.58%, respectively.
Points of comparison	Leakage power, Delay, PDP
Software	Mentor Graphics tools
Node	16 nm FinFET
Circuits	- NAND GATE - NOR GATE -C17 benchmark circuit
Limitations	The study is limited to simulation results under specific conditions, without experimental validation or analysis of large-scale circuit implementations.

11. ***Study of the Reliability for the Leakage Mitigation Methods using FinFETs***	
Authors	- Ms. Kajal - Vijay Kumar Sharma
Year	2023
Summary	*Investigation of various leakage mitigation techniques in FinFET technology, focusing on their reliability under process, voltage, and temperature (PVT) variations. *Analysis of leakage reduction techniques like **ONOFIC, alternative ONOFIC, Cascaded Leakage Control Transistor (CLCT)**, and others in footer-less domino logic (FLDL) circuits. *Results showing that the **CLCT approach** offers the best reliability and the lowest power dissipation under PVT variations. *Discussion of the influence of process variations on leakage current, power dissipation, and overall circuit performance.
Points of comparison	Leakage current, Power Dissipation, Delay
Software	Cadence Virtuoso
Node	16nm FinFET
Circuits	- Footer-less Domino Logic (FLDL) OR2 circuit

	- Various domino logic circuits, including FDSTDL and DNDFTDL.
Limitations	The paper primarily examines leakage current mitigation techniques. Other critical performance aspects, such as timing optimization, noise resilience, and power distribution networks, are not extensively covered

12. 1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications	
Authors	- Chandra Shaker Pittala - Vallabhuni Vijay - B. Naresh Kumar Reddy
Year	2023
Summary	*To improve performance by reducing propagation delay and power dissipation in multi-bit arithmetic circuits *The carry cells presented in the paper reduce total transistor usage and minimize the silicon area required for the carry circuits. **Eight new full adder circuits** based on the proposed carry cells are compared with existing designs, showing improved performance of *Evaluating TGA,SCMOS,HCMOS,BBL & CPL in terms of power delay product (PDP), delay, and power consumption. *The performance of an 8-bit Ripple Carry Adder (RCA) circuit constructed with these proposed cells, showing lower delay compared to traditional RCA designs.
Points of comparison	1.Delay 2. Power consumption 3. Power Delay Product
Software	Cadence Virtuoso
Node	18 nm FinFET
Circuits	- Full adder carry circuits - Ripple Carry Adder (RCA)
Limitations	-The focus is mainly on carry cells and full adder circuits. Other essential arithmetic circuits like multipliers and dividers were not explored in detail -The performance analysis is based on specific load conditions and voltage ranges (0.4V–1.8V), and the circuits may behave differently under varying real-world conditions such as higher loads or more dynamic voltage scaling.

Chapter 1

Introduction

1.1 What is FinFET?

A Fin Field-Effect Transistor (FinFET) is a type of non-planar, multi-gate transistor used in modern semiconductor devices. Unlike traditional planar MOSFETs, which have a single gate on top of a flat channel, FinFETs feature a three-dimensional structure where the channel is formed on a thin silicon fin that protrudes from the substrate. The gate wraps around the fin on three sides—top and both vertical sidewalls—providing better control over the channel and significantly reducing short-channel effects **[1]**. The improved gate control in FinFETs allows for lower leakage currents, higher switching speeds, and better performance at smaller technology nodes, typically below 32 nanometers **[2]**. FinFETs can be manufactured in single-gate, double-gate, or tri-gate configurations, with tri-gate being the most common in industry-standard devices due to its superior electrostatic behavior **[2]**.

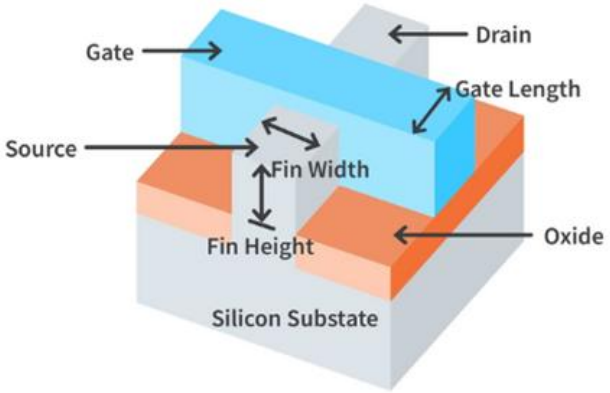


Figure 1.1 : FinFET

1.2 Basic Functionalities of FinFET

FinFETs function as voltage-controlled current devices, similar to traditional MOSFETs, but with enhanced electrostatic control and performance due to their 3D structure. The basic functionalities of a FinFET are as follows:

1. **Switching Behavior:** FinFETs operate as electronic switches that turn ON or OFF depending on the gate voltage. When the gate voltage exceeds the threshold voltage, an inversion layer forms along the sides and top of the fin, allowing current to flow between

the source and drain. When the gate voltage is below the threshold, the current path is effectively blocked, switching the transistor OFF.

2. **Gate Control:** The most notable feature of FinFETs is their multi-gate structure. The gate wraps around the fin and provides better electrostatic control over the channel compared to the planar MOSFET. This reduces short-channel effects and improves the subthreshold slope, enhancing switching performance and reducing leakage **[1][2]**.

3. **Current Conduction:** In FinFETs, current flows through the vertical fin or channel. The effective channel width is determined by the height of the fin and the number of fins used in parallel. By increasing the number of fins, the drive current can be scaled up to meet circuit performance requirements.

4. **Threshold Voltage Modulation:** FinFETs allow for better control and tuning of threshold voltage (V_th) through channel doping and gate work function engineering. This enables designers to optimize performance and power consumption for specific applications.

5. **Scalability and Density:** Due to their vertical structure and improved electrostatics, FinFETs can be scaled down more effectively than planar devices. This enables higher transistor density, which is essential for modern integrated circuits that demand more functionality in less area **[2]**.

6. **Reduced Leakage:** The tri-gate structure minimizes leakage currents when the device is in the OFF state. This significantly reduces static power consumption, which is especially important for battery-powered and high-density computing devices.

FinFETs perform the same basic switching and amplification roles as MOSFETs but with improved characteristics, enabling their use in high-performance and low-power digital systems.

1.3 Different Aspects of FinFET

FinFET technology introduces several key structural and electrical improvements over traditional MOSFETs, which affect various aspects of device behavior, design, and performance. The major aspects of FinFETs are discussed below:

1. **Structural Aspect:** FinFET is built with a thin silicon fin that rises perpendicularly from the Si substrate. The gate electrode wraps around the fin on three sides: top and two vertical sidewalls forming a tri-gate structure. This 3D architecture helps to increase the effective channel width and provide superior gate control which is essential for minimizing short channel effects as the devices shrink.

2. **Electrical Aspect:** The 3D gate structure helps to improve the sub-threshold slope, reduce drain induced barrier lowering (DIBL) and suppress leakage current. By this, it

results in better switching characteristics with lower static power consumption. FinFETs also support operation at lower threshold voltages enhancing the overall energy efficiency **[2]**.

3. **Performance Aspect:** FinFET offers higher drive current due to the increased effective channel width per unit footprint. This leads to faster switching speeds which is a very critical task for high performance digital circuits. It also demonstrates better scalability continuing transistor miniaturization at nodes below 32 nm **[2]**.

4. **Fabrication Aspect:** Fabricating FinFET devices involves a complex process than planar MOSFETs such as fin patterning, gate wrapping and precise control of doping. Modern lithography and etching techniques are used to ensure uniform fin height and width. Apart from the complexity, FinFET manufacturing has become matured enough and is widely adopted in commercial foundries as well.

5. **Power Aspect:** FinFETs can significantly reduce leakage power which is a major issue in deep Submicron technology. Their capability to operate at a lower supply voltages also contributes to reduced dynamic power consumption making them ideal for low powered applications such as mobile devices and data centers.

6. **Design Aspect:** Designing the devices/ICs with FinFETs requires consideration of quantized fin widths, discrete drive strengths and fin alignment with layout rules. Electronic Design Automation (EDA) tools have evolved to support FinFET specific design constraints enabling effective integration into digital design flows.

1.4 Types of FinFET

Based on the underlying substrate used during fabrication, FinFETs are fundamentally classified into two types: **Bulk FinFET** and **SOI (Silicon-On-Insulator) FinFET**. The choice of substrate impacts the device performance, power consumption, isolation characteristics, and manufacturing complexity.

1.4.1 Bulk FinFET

Bulk FinFET can be fabricated directly on a standard bulk silicon substrate wafer. This type of FinFET uses shallow trench isolation (STI) and well doping techniques to isolate the fins and control the leakage flow. Bulk FinFETs are attractive as they are compatible with traditional CMOS fabrication processes which make them easier and cheaper to produce at scale. Due to the direct contact with the substrate, however, there is a higher possibility of junction leakage which can impact the power efficiency.

***Advantages**:*
– Lower manufacturing cost
– High compatibility with existing CMOS processes

– Easier integration into large-scale production

Disadvantages:
– Increased leakage due to substrate coupling
– Slightly weaker electrostatic control compared to SOI FinFETs

1.4.2 SOI FinFET (Silicon-On-Insulator FinFET)

SOI FinFETs are built on a layered substrate that includes a thin insulating layer (typically silicon dioxide) between the silicon fin and the underlying bulk substrate. This insulating layer effectively reduces parasitic capacitance and leakage current. SOI FinFETs provide better isolation and superior electrostatic control, especially beneficial for low-power and high-speed applications.

Advantages:
– Strong electrical isolation
– Lower leakage current
– Improved subthreshold performance

Disadvantages:
– Higher wafer and fabrication cost
– Limited availability of SOI substrates compared to bulk

Aspect	Bulk FinFET	SOI FinFET
Substrate	Bulk silicon	Silicon-on-insulator (SiO_2 layer)
Electrical Isolation	Moderate	Strong (due to buried oxide)
Leakage Current	Higher	Lower
Manufacturing Cost	Lower	Higher
CMOS Compatibility	High	Moderate
Performance at Low Power	Moderate	Better due to reduced parasitics

Table 1.1: Distinction Between Bulk and SOI FinFETs

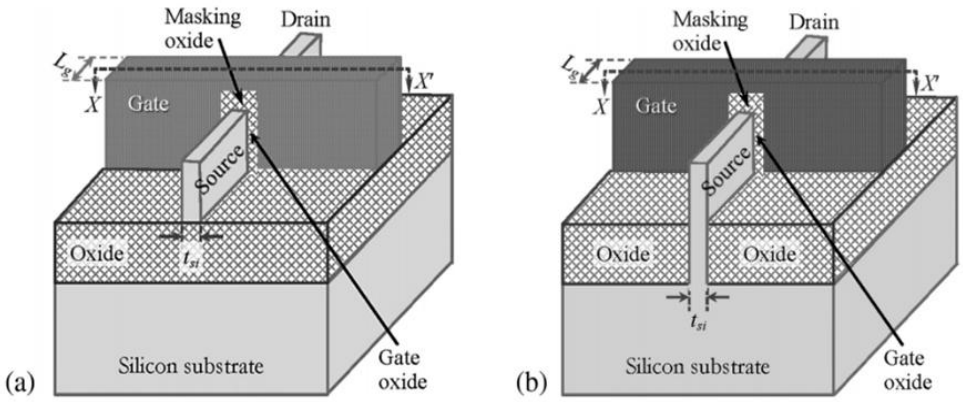


Figure 1.2 Bulk and SOI FinFET

1.5 Background and Motivation behind using FinFET :

As semiconductor technology progresses into the nanometer regime, particularly below the 32 nm node, conventional planar MOSFETs face severe limitations due to short-channel effects (SCEs) **[2]**. These effects degrade the performance and energy efficiency of transistors, making it increasingly difficult to scale down devices while maintaining desired electrical characteristics. The fundamental issues include:

Drain-Induced Barrier Lowering (DIBL): In short-channel MOSFETs, a high drain voltage can lower the potential barrier at the source-channel junction, allowing electrons to flow even when the gate voltage is low. This leads to unwanted leakage and poor control over the channel.

Threshold Voltage Roll-Off: As channel lengths shrink, the threshold voltage (V_th) at which a transistor turns on becomes less predictable and tends to decrease. This results in inconsistent switching behavior and affects circuit reliability.

Degradation of Subthreshold Slope (SS): A degraded subthreshold slope means that the transition from OFF to ON state is not sharp. This weakens the gate's ability to control the channel and increases power consumption in standby modes.

Increased Leakage Current: A less steep subthreshold slope also contributes to higher leakage current, which is particularly problematic in low-power applications where energy efficiency is critical.

These limitations require a shift from planar MOSFETs to a more robust device architecture FinFET (Fin Field-Effect Transistor). FinFETs employ a three-dimensional fin-like structure, allowing the gate to wrap around the channel on multiple sides. This multi-gate configuration enhances gate control, reduces SCEs, and enables effective scaling below 32 nm **[2]**.

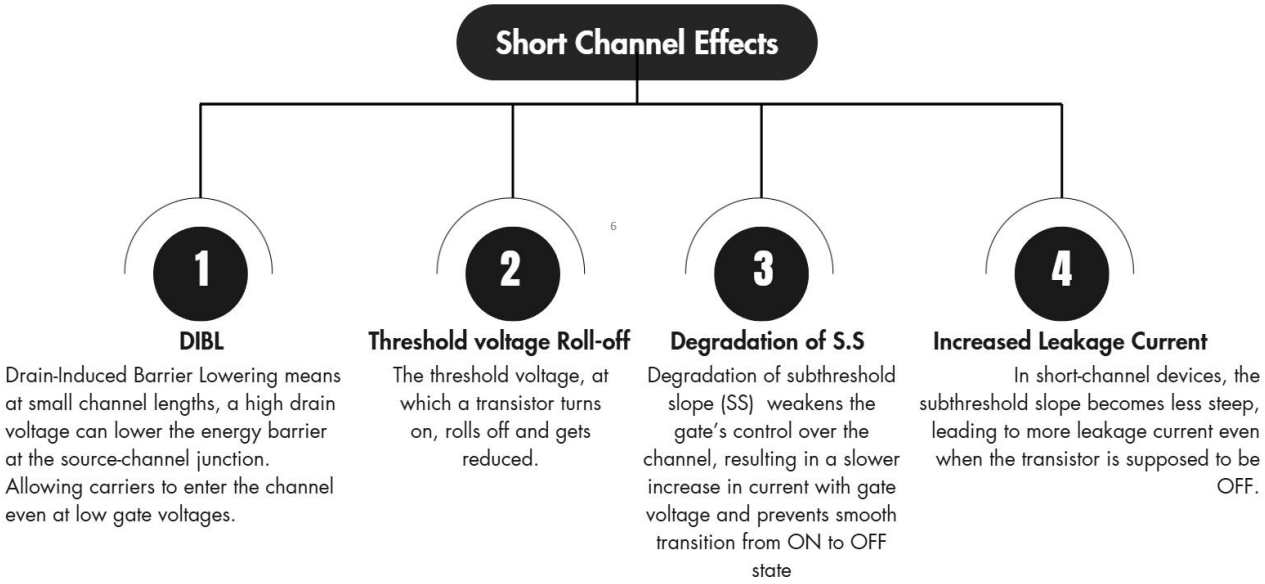


Figure 1.3 Short Channel effects

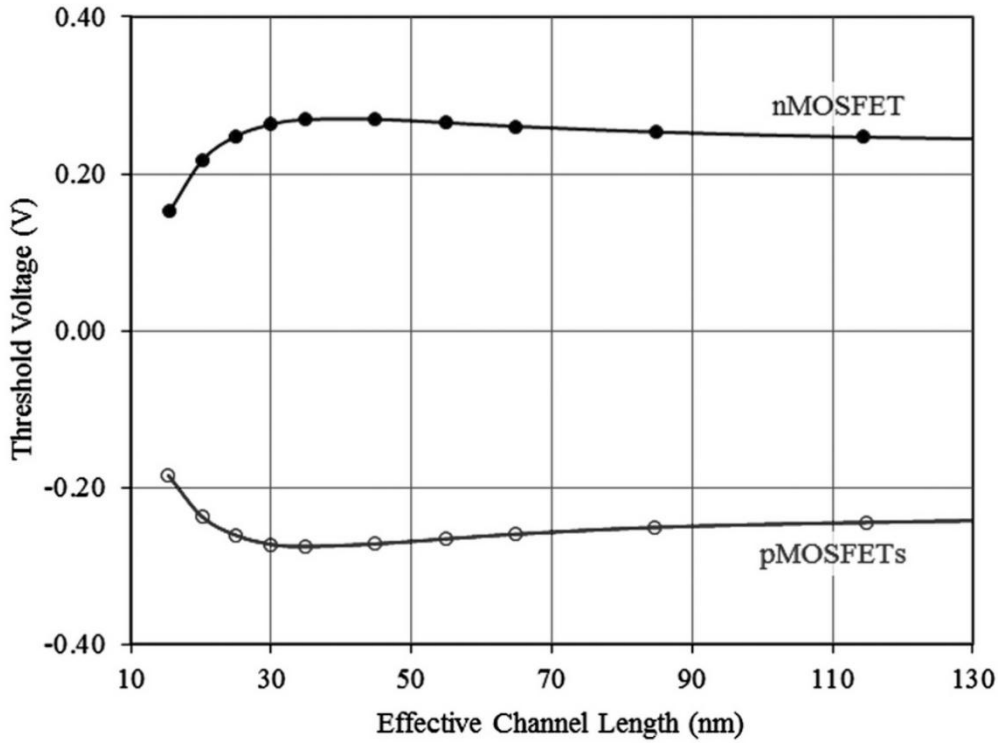


Figure 1.4: Decrease of Vth with decrease of channel length

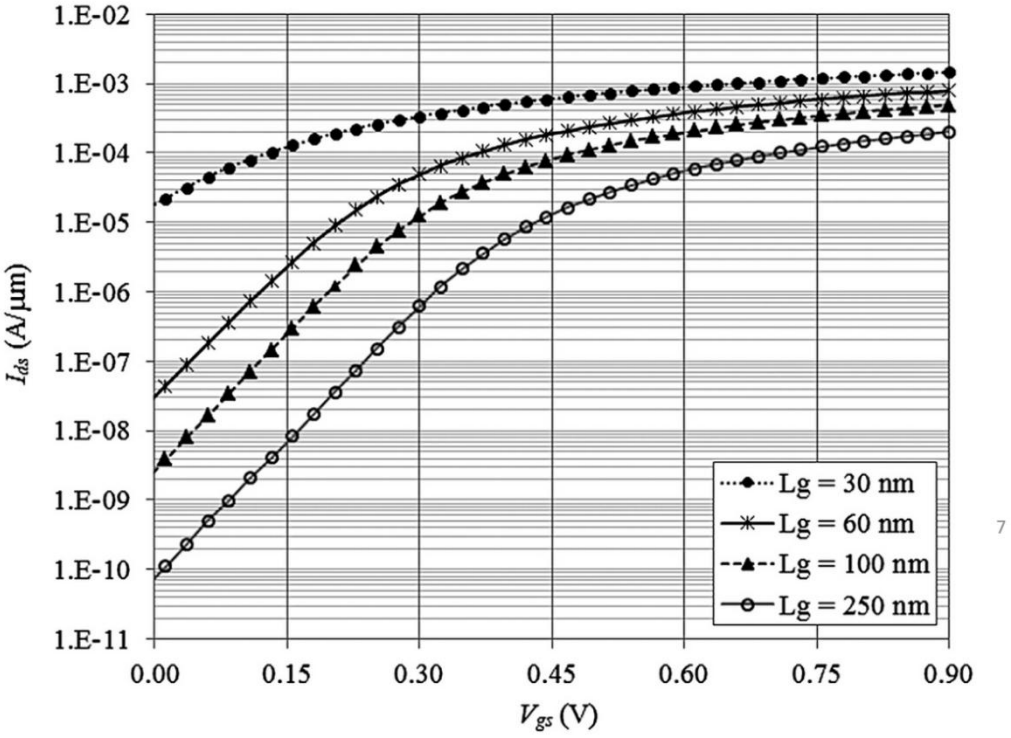


Figure 1.5 Drain current (Ids) vs Gate Voltage (Vth) for a planar MOSFET

In the figure above, it can be seen that with the decrease in channel length the I_ds–V_g curve becomes less and less steep, indicating the prominence of short-channel effects.

The motivation for using FinFETs in digital circuit design includes:

Improved Short-Channel Control: FinFETs significantly suppress DIBL and threshold voltage roll-off, ensuring reliable operation at small geometries **[1]**.

Lower Leakage Power: The superior gate control reduces subthreshold leakage, which is a major contributor to static power in modern ICs **[2]**.

Better Performance: FinFETs provide higher drive current and faster switching due to increased effective channel width and reduced parasitic capacitances **[1]**.

Enhanced Scalability: The 3D geometry of FinFETs allows for continued transistor scaling in accordance with Moore's Law, which is essential for increasing transistor density in VLSI systems **[2]**.

Therefore, FinFET-based circuits are becoming the standard for high-performance and low-power digital applications, making them an essential area of research and implementation in modern VLSI and IC design.

Chapter 2

Overview of Device Simulation

2.1 Introduction

For simulating the device and analyzing its device physics we have used the Silvaco TCAD tool. The version used was Silvaco TCAD 2019.

Silvaco TCAD (Technology Computer-Aided Design) is a very useful suite of simulation tools used for modeling and analysis of semiconductor devices. It allows us to simulate the fabrication process and electrical behavior of devices like MOSFETs, FinFETs, and advanced nanoscale structures. For process simulations the ATHENA tool is very handy and ATLAS is used for device simulation purposes. Silvaco TCAD provides a detailed understanding of device physics.

FinFET is a 3D device, therefore the device modelling and simulation also had to be in 3D. For generating the 3D structure the DEVedit tool was used. The simulator used was ATLAS which is the physics engine of the Silvaco TCAD 2019.

2.2 Device Simulation

We chose to resimulate a FinFET device from an existing article from 2022 **[8]**.

2.2.1 Device Structure

Parameters	**Values**
Channel length, *Lg*	20nm
Fin height, *Hfin*	26nm
Fin width, *Wfin*	6.5nm

S/D length, LS/D	50 nm
S/D extension length, LS/D	7nm
Buried oxide (SiO2) thickness, tBOX	50 nm
Gate dielectric (HfO2) thickness, tox	4nm
Channel doping (boron, p-type), Nch	10^{16} cm^{-3}
S/D doping (arsenic, n-type), NS/D	10^{21} cm^{-3}
S/D extension doping (arsenic, n-type)	10^{19} cm^{-3}
Si substrate thickness	50 nm
Si substrate doping (boron, p-type)	10^{16} cm^{-3}
Gate work function (TiN (Sn), Φm)	4.32eV

Table 2.1: Device Parameters

These parameters correspond to a modern FinFET device structure and were used to calibrate our simulations. By using a known device setup from literature **[8]**, we ensured that our simulation framework could reproduce expected device characteristics before exploring new design ideas.

2.2.2 Simulation Profile

For simulating the electrical behavior of the device, the Source and the Bulk terminals were grounded. VSource=0 and VBulk=0

The drain voltage, VDrain was fixed at 0.05V

The Gate voltage, VGS was swept from 0 to 1V

The step size for the VGS sweep was 0.125V

The Drain to source current was recorded for the sweep.

The solver used for the simulation was Automatic Newton-Raphson with max number of bias step reduction for a single point set to 20.

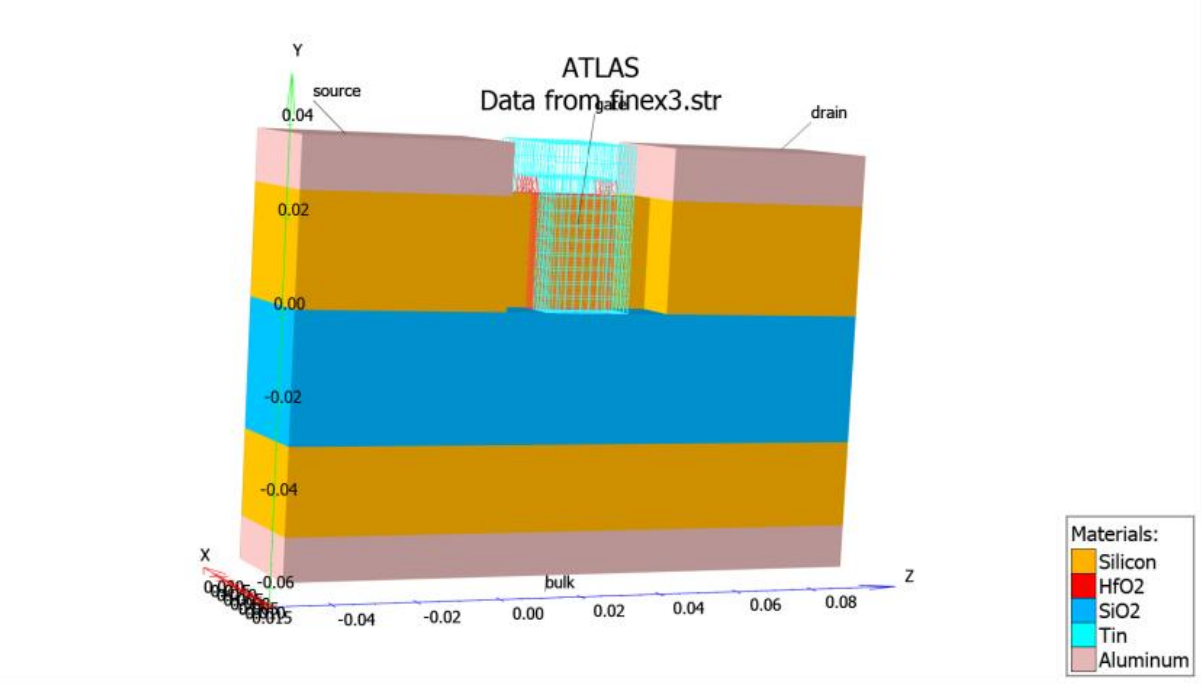


Figure 2.1: Device Structure

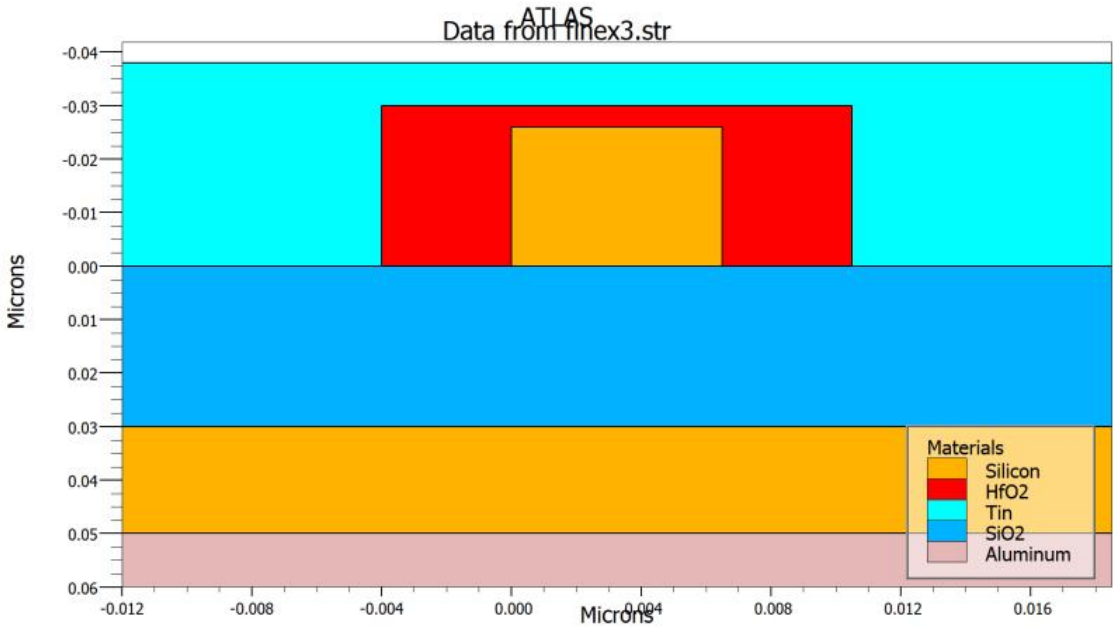


Figure 2.2: Device Cross-Section

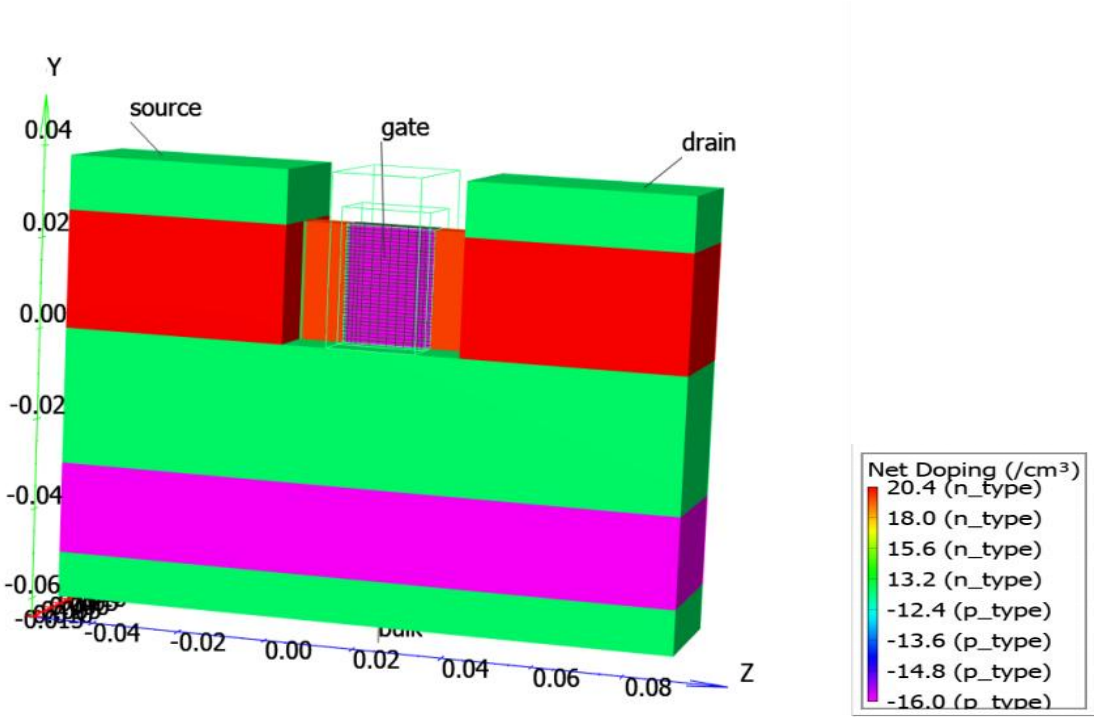


Figure 2.3: Device Doping Profile (3D View)

2.2.3 Physics Models

SCVT Model
The SCVT (Slotboom-Carrier-Voltage-Temperature) model is used to model concentration-dependent mobility. It simulates the effects of doping concentration, temperature, and electric field. This is for ensuring realistic carrier transport in regions with high doping gradients.

CCSMOB Model
The CCSMOB (Concentration and Carrier-Scattering Mobility) model includes carrier-carrier and carrier-impurity scattering mechanisms. It adjusts mobility based on carrier concentration and electric field.

ANALYTIC Model
This model provides analytical expressions for field- and temperature-dependent mobility. It simplifies simulations while maintaining reasonable accuracy, making it efficient for compact device modeling.

BGN (Band Gap Narrowing)
The BGN model accounts for bandgap reduction at high doping levels, affecting intrinsic carrier concentration and thus altering device characteristics in heavily doped regions.

Shockley-Read-Hall (SRH) Recombination
This physics model defines recombination via defect levels. The recombination rate is:

$$R_{SRH} = \frac{np - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}$$

R_{SRH}: Recombination rate.

n_p: Electron and hole concentrations.

n_i: Intrinsic concentration of carriers

τ_n, τ_p : Lifetime duration of electrons and holes.

n_1, p_1: Trap-dependent terms

Auger Recombination
This model captures high-density carrier effects where recombination transfers energy to a third carrier:

$R = C_n \cdot n^2 \cdot p + C_p \cdot n \cdot p^2$

Fermi–Dirac Distribution
Used instead of Maxwell-Boltzmann statistics under high doping or low temperature. Carrier occupation probability:

$f(E) = 1 / (1 + \exp[(E - E\_F) / kT])$

BQP (Bohm Quantum Potential)
This model includes quantum confinement by adding a quantum potential term to transport equations. It captures energy sub-band shifts and spatial carrier confinement effects, especially in nano-scale devices.

FLDMOB Model
The FLDMOB (Field Dependent Mobility) model accounts for the reduction in carrier mobility as the electric field increases, which is significant in high-field regions like MOSFET channels. It models velocity saturation due to increased carrier scattering. The field-dependent mobilities are:

$\mu_n = \mu_n D / (1 + 1.54 \times 10^{-5} \cdot E)$
$\mu_p = \mu_p D / (1 + 5.35 \times 10^{-5} \cdot E)$

Here, $\mu_n D$ and $\mu_p D$ are low-field mobilities for electrons and holes, and E is the electric field.

Chapter 3

Device Simulation Results and Analysis

3.1 Physical Profile of the device

We took a cutline along the z-axis from source to drain with the channel in the middle; variation of different properties along this line is visualized in the following graphs.

Net Doping:

x-axis: position(microns),

y-axis: net doping concentration/cm3 (logarithmic)

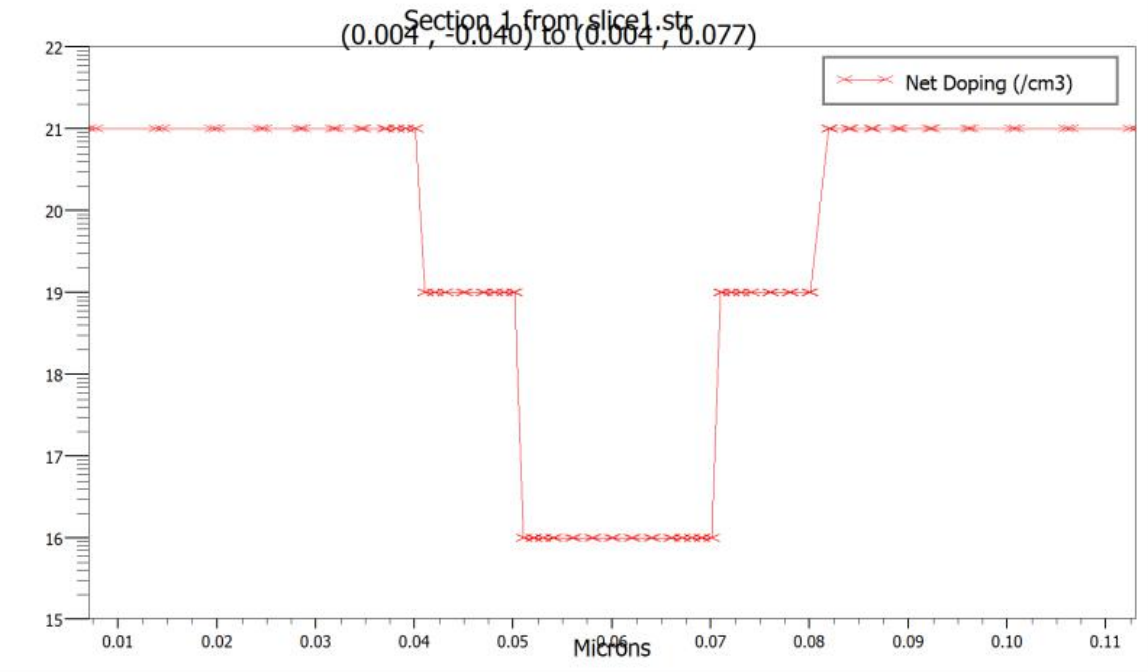


Figure 3.1: Net Doping along Source to Drain Axis

Electron Concentration:

x-axis: position(microns),

y-axis: electron concentration (linear)

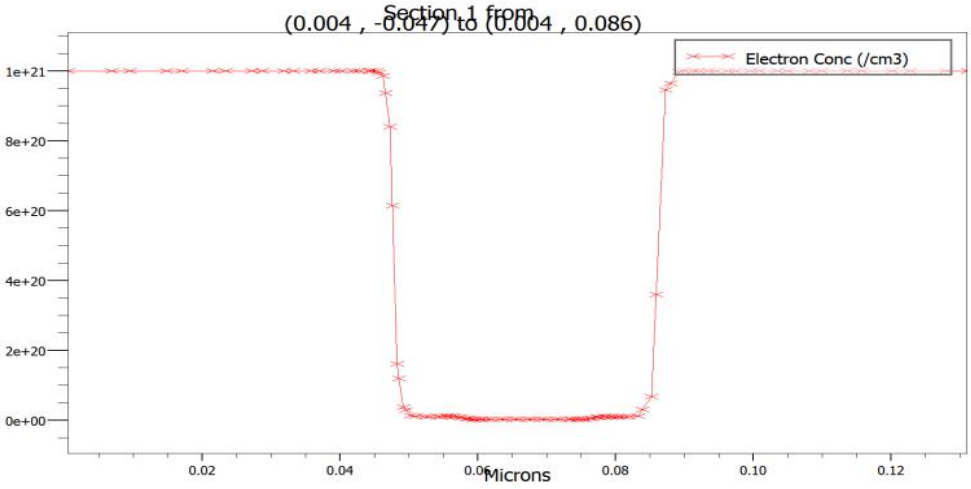


Figure 3.2: Electron Concentration along Source to Drain Axis

Hole Concentration:

x-axis: position(microns),

y-axis: hole concentration/cm3 (linear)

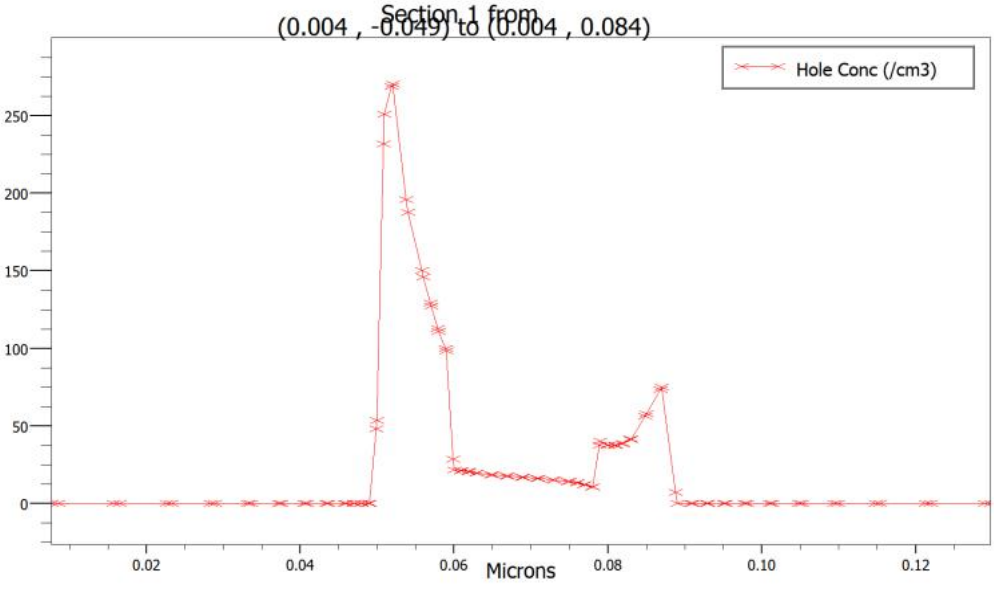


Figure 3.3: Hole Concentration along Source to Drain Axis

3.2 Transfer Characteristics

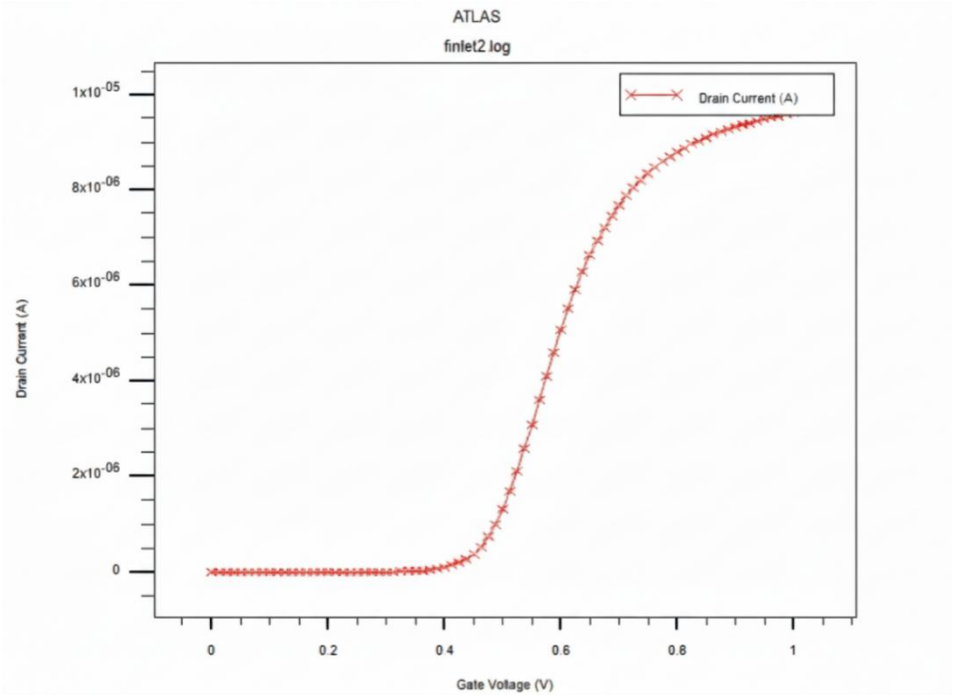


Figure 3.4: IDS vs VGS curve (Not Normalized)

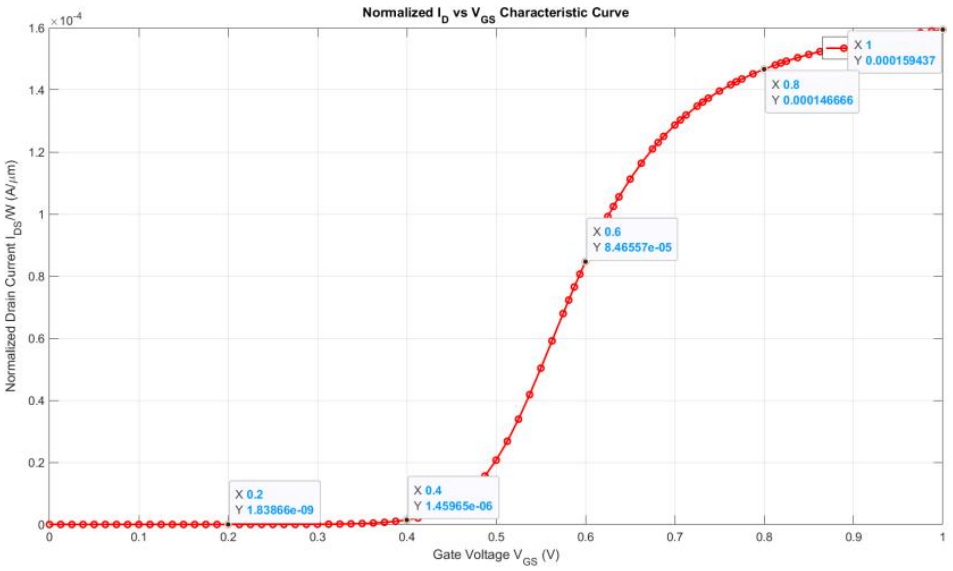


Figure 3.5: IDS vs VGS curve (Normalized)

3.3 Result Analysis

Effective Channel Width, $W = 2H_{fin} + W_{fin}$

The Drain-to-Source current has been normalized by the Effective Channel width.

From the normalized data, using the constant current method (IDS>1uA/um for VGS>Vth), we found the threshold voltage to be:

Threshold Voltage, Vth= 0.375V

VGS<Vth is the subthreshold region and the subthreshold slope was calculated using the formula:

$$SS = \frac{d(V_{gs})}{d[log(I_{ds,sat})]}$$

Subthreshold slope was found to be 65.15mv/decade.

The Subthreshold slope has a theoretical limit for FinFET devices, which is 60mV/decade.

I_{DS} saturates at V_{DS} = 0.8V (approximately)

$V_{DS\ (Sat)}$ = 0.8V

Chapter 4

Circuit Simulation

4.1 Environment Setup

All circuit simulations were performed using the Cadence Virtuoso Software with the Spectre SPICE simulator engine.

PTM SPICE models developed by University of Arizona were used for simulating the Bulk-CMOS and the FinFET Circuits. PTM 32nm Bulk_CMOS and PTM 7nm FinFET model files were used.

The CNFET model used is the VS-CNFET Verilog-A model developed jointly by Stanford University and MIT.

For both p-type and n-type devices:

Bulk-CMOS Channel Length: 32nm
FinFET Channel Length: 10nm
CNFET Channel Length: 10nm

Channel Widths:

P-CMOS: 120nm
N-CMOS: 60nm

P-FinFET: *Effective Width*: 85nm
N-FinFET: *Effective Width*: 42.5nm

P-CNFET: 1 CN Tube, *diameter*: 1nm
N-CNFET: 1 CN Tube, *diameter*: 1nm

PMOS and P-FinFET widths have been chosen twice that of NMOS and N-FinFET widths because the P-type devices have half the carrier mobility of the N-type Devices. Scaling the widths balances this ensuring equal conduction capacity of the devices.

CNFET CN Tube (Carbon Nano Tube) diameter is same for P-type and N-type devices because the devices are completely symmetric and the carbon nano-tube channel is same for both devices.

4.2 SPICE Models

4.2.1 CMOS SPICE Model

PTM 32nm Bulk CMOS Model:

The PTM 32 nm Bulk CMOS model represents one of the mature technology nodes in the predictive model series, serving as a standard benchmark for bulk planar transistor-based designs. It captures the device physics of conventional CMOS transistors fabricated on bulk silicon substrates. The model includes critical short-channel effects such as threshold voltage roll off, channel length modulation, and subthreshold leakage current. PTM 32 nm parameters are derived from the foundry data which are intended to predict the device characteristics consistent with realistic fabrication processes. This model basically uses BSIM-4 since its core compact model framework incorporating temperature dependent effects and process variations to enhance simulation accuracy. It is an essential reference point for comparing the evolution of device characteristics from planar CMOS to FinFET and CNFET architectures. The PTM 32 nm Bulk CMOS model is used particularly for evaluating the limitations of conventional MOSFET scaling with understanding leakage and power dissipation trends in pre FinFET era technologies.

4.2.2 FinFET SPICE Model

PTM 7nm SPICE Model:

Predictive Technology Model (PTM), 7 nm SPICE model, is a widely adopted compact model for simulating nanoscale FinFET technologies developed by Arizona State University. This model provides with a predictive framework for circuit designers to analyze device behavior at the sub 10 nm regime where short channel effects, quantum mechanical tunneling and non ideal gate control become a dominant phenomena. The PTM 7 nm model incorporates advanced physical effects such as gate leakage, drain-induced barrier lowering (DIBL), and velocity saturation. It is based on multi-gate transistor structures, which provide better electrostatic control over the channel and significantly reduce leakage currents compared to the planar MOSFETs. The model parameters are calibrated using both the empirical data and the theoretical projections to make sure consistency with the International Technology Roadmap for Semiconductors (ITRS) projections for 7 nm node devices. Due to its balance between accuracy and computational efficiency, the PTM 7 nm FinFET model is extensively used for low powered VLSI design allowing circuit researchers to simulate and optimize power, delay and leakage characteristics.

4.2.3 CNFET SPICE Model

Stanford-MIT VS-CNFET Model:
The Stanford MIT Virtual Source Carbon Nanotube Field Effect Transistor (VSCNFET) model is an advanced physics based compact model designed for circuit level simulation of emerging carbon nanotube transistor technologies. The model developed collaboratively by Stanford University and the Massachusetts Institute of Technology, captures the unique carrier transport properties of carbon nanotubes such as quasi-ballistic conduction and one dimensional electron transport. Unlike the conventional MOSFET models, it employs a virtual source approach where the current is modeled based on carrier injection velocity and potential barrier modulation near the source channel interface. This methodology allows an accurate representation of short channel effects and velocity saturation phenomena. The model supports multiple parameters including tube diameter, contact resistance and mean free path enabling detailed exploration of performance tradeoffs. It also accounts for the parasitic capacitances and quantum confinement effects making it highly suitable for simulating low powered, high-speed nanoscale digital circuits. The Stanford MIT VSCNFET model has been extensively validated against experimental data and widely used in research to evaluate CNFET based circuit architectures comparing their performance to FinFET and CMOS counterparts.

4.3 Circuits Chosen for Simulation

4.3.1 Inverter

The inverter or NOT gate is the simplest and most fundamental logic circuit. It consists of a single-stage complementary pair of transistors typically an n-type and a p-type device configured such that the output is always the logical complement of the input. In CMOS and FinFET technologies, when the input is logic '1', the n-type device conducts while the p-type device remains off, pulling the output to logic '0'. Conversely, when the input is logic '0', the p-type transistor conducts and drives the output to logic '1'. This complementary switching action results in very low static power dissipation, as only leakage current flows in the steady state.

Input (A)	Output (Y)
0 → 1	1 → 0

Table 4.1: Inverter Truth Table

The inverter is highly suitable for technology comparison because it directly reflects the intrinsic delay, switching energy, and leakage current behavior of individual transistors. Its simplicity eliminates the influence of logic complexity, isolating the effects of the underlying

device characteristics. Therefore, it is often used as a reference circuit for evaluating new device models and leakage reduction techniques such as LECTOR and INDEP.

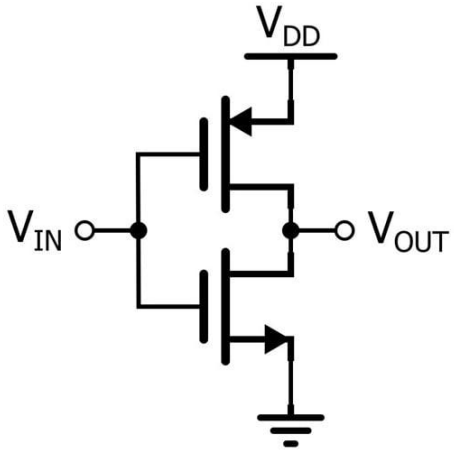


Figure 4.1: CMOS Inverter Schematic

4.3.2 NAND

The NAND gate is an universal logic gate that outputs a low logic level only when all inputs are high. It consists of a combination of series and parallel transistor networks. In a 2-input CMOS NAND gate, the pull-down network consists of two nMOS transistors in series while the pull-up network has two pMOS transistors in parallel. This configuration ensures a low output resistance in logic '1' states and high resistance in logic '0' states.

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 4.2: NAND Truth Table

The NAND gate is particularly valuable for the technology comparison as it introduces both series and parallel transistor conduction paths revealing how a technology handles stacking effects, short channel behavior and drive capability under different input combinations. Its structure amplifies the influence of leakage mitigation techniques as multiple transistors interact in both active and idle states. As a result, the NAND gate offers meaningful insights into dynamic power consumption, propagation delay and leakage current control efficiency.

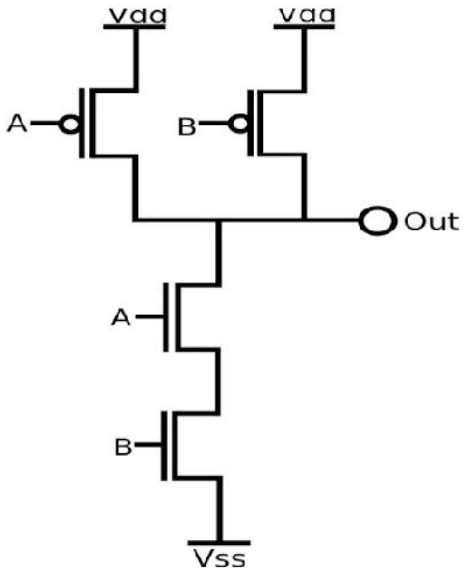


Figure 4.2: CMOS NAND Schematic

4.3.3 NOR

NOR gate (NOT with OR) is another universal gate that outputs a logic high only when all inputs are low or '0'. In a 2-input CMOS NOR gate, the pull-up network consists of pMOS transistors in series while the pull-down network has nMOS transistors in parallel. This configuration contrasts with the NAND gate which leads to slower pull-up transitions due to the series-connected pMOS devices. Consequently, the NOR gate generally exhibits higher delay and power consumption than the NAND gate in most CMOS technologies.

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

Table 4.3: NOR Truth Table

The NOR gate's structural asymmetry makes it a strong candidate for analyzing p-type transistor performance and the impact of leakage reduction schemes on pull-up networks. Because NOR gates emphasize the behavior of pMOS (or p-FinFET / p-CNFET) devices under stacked configurations, they complement NAND gate analysis, providing a complete performance profile of a given technology. Hence, the inverter, NAND, and NOR gates together form a representative suite for benchmarking device technologies and evaluating the effectiveness of leakage optimization techniques.

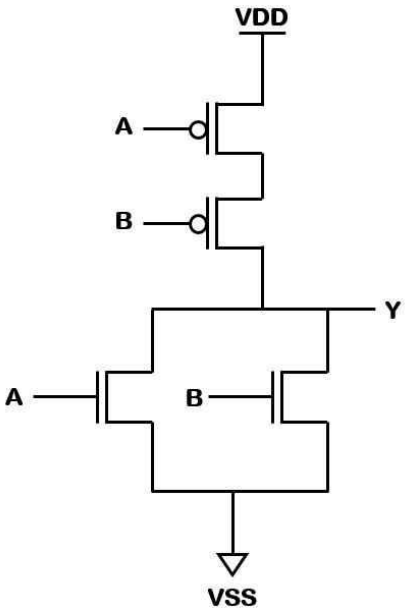


Figure 4.3: CMOS NOR Schematic

4.4 Performance Metrics

4.4.1 Propagation Delay

Propagation delay (t_{pd}) is defined as the time required for an input signal transition to cause a corresponding change in the output voltage of a circuit. It represents the intrinsic switching speed of a logic gate and directly influences the overall operating frequency of a digital system.
Mathematically, propagation delay is expressed as:

$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2}$$

where t_{PLH} is the delay from a low-to-high transition, and t_{PHL} is the delay from a high-to-low transition at the output. In physical terms, propagation delay depends on parameters such as channel length, drive current capability, load capacitance, and parasitic resistances. Technologies like FinFETs and CNFETs offer reduced channel resistance and improved gate control, minimizing delay compared to planar CMOS **[2]**. Lower propagation delay implies faster switching, but aggressive scaling may increase leakage and dynamic power, creating a power–speed trade-off.

4.4.2 Static Leakage

Static leakage power arises from unwanted current flow when a transistor is in its non-conducting or idle state. Due to subthreshold conduction, gate oxide tunneling, and junction leakage, a small leakage current flows even when the transistor is logically off.
The static leakage power is given by:

$$P_{static} = I_{leakage} \times V_{DD}$$

where $I_{leakage}$ is the total leakage current and V_{DD} is the supply voltage **[3]**. As device dimensions shrink to nanometer scales, short-channel effects and reduced threshold voltage exacerbate leakage **[3]**. Techniques such as LECTOR, INDEP, and MTCMOS help reduce leakage without degrading performance. Static leakage is critical for standby-mode circuits and battery-powered systems.

4.4.3 Average Power

Average power consumption (P_{avg}) basically evaluates the total energy dissipated by a circuit during a complete switching cycle. It consists of both the dynamic and the static power components.

$$P_{avg} = P_{dynamic} + P_{static}$$

The dynamic power component is arised from capacitive charging and discharging during logic transitions and is given by:

$$P_{dynamic} = \alpha \times C_L \times V_{DD}^2 \times f$$

Here, α is the activity factor. C_L is the effective load capacitance and f is the clock frequency **[3]**. Average power determines the thermal reliability and energy efficiency of the circuit. In modern designs, both the dynamic and the static components must be optimized simultaneously to achieve low power operation.

4.4.4 Power Delay Product (PDP)

The Power Delay Product (PDP) is a key parameter that combines power consumption and delay to represent the energy consumed per switching event. It can be defined as:

$$PDP = P_{avg} \times t_{pd}$$

A lower PDP depicts higher energy efficiency and faster operation. It is used particularly when comparing different device technologies or leakage optimization techniques. FinFET and CNFET technologies generally exhibit lower PDP values due to improved electrostatic control, reduced leakage and higher drive current **[2]**. Thus, PDP provides an effective measure of the tradeoff between speed and power efficiency.

4.5 Cadence Virtuoso Circuit Schematics

The Circuit Schematic Diagrams designed in Cadence Virtuoso for simulation:

Inverter Circuit:

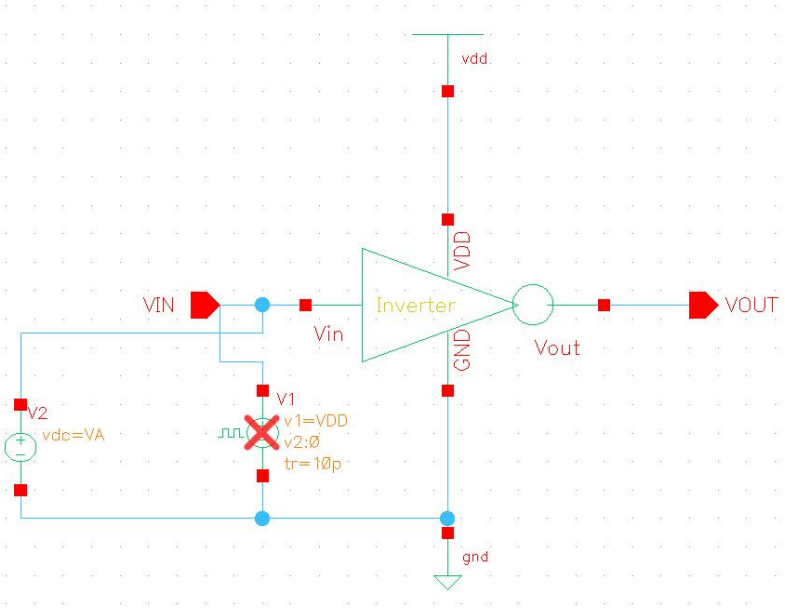


Figure 4.4: Inverter Test Setup

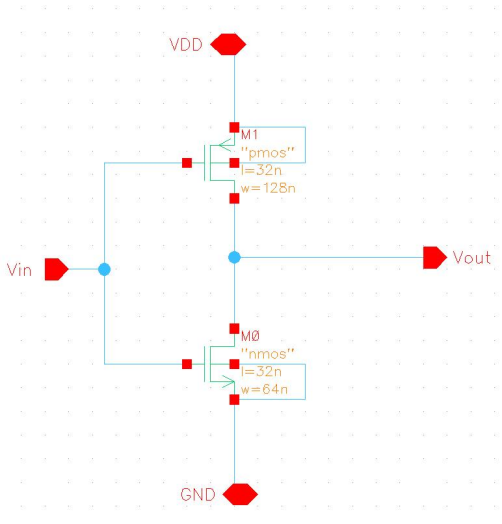


Figure 4.5: Inverter Schematic

NAND Circuit:

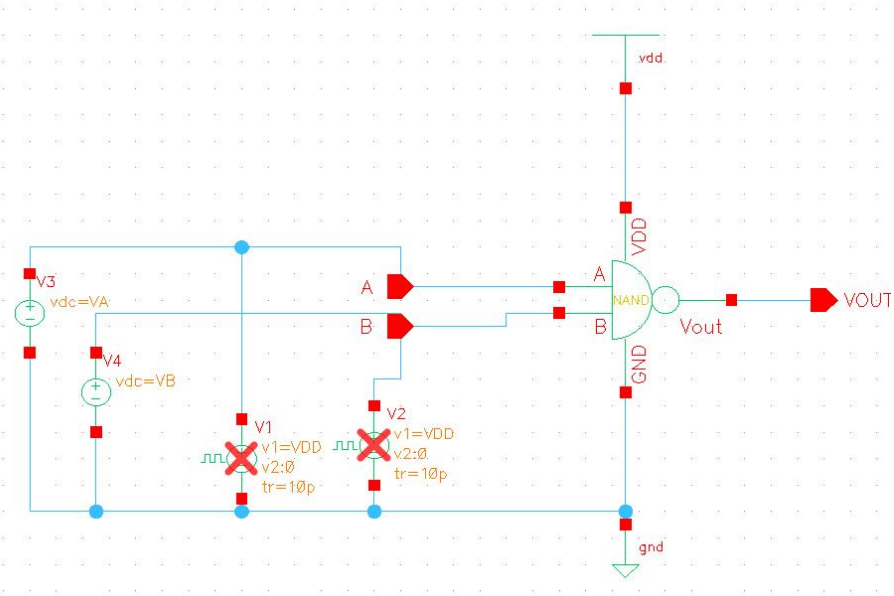


Figure 4.6: NAND Test Setup

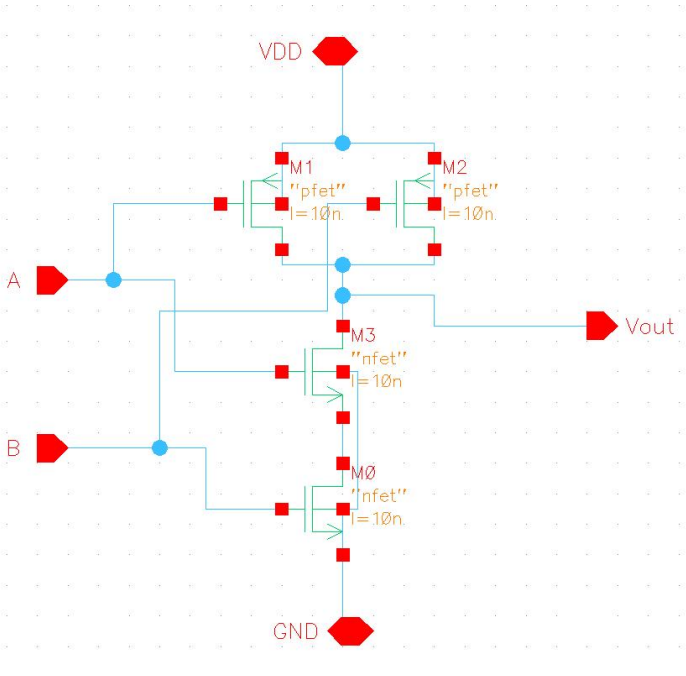


Figure 4.7: NAND Schematic

NOR Circuit:

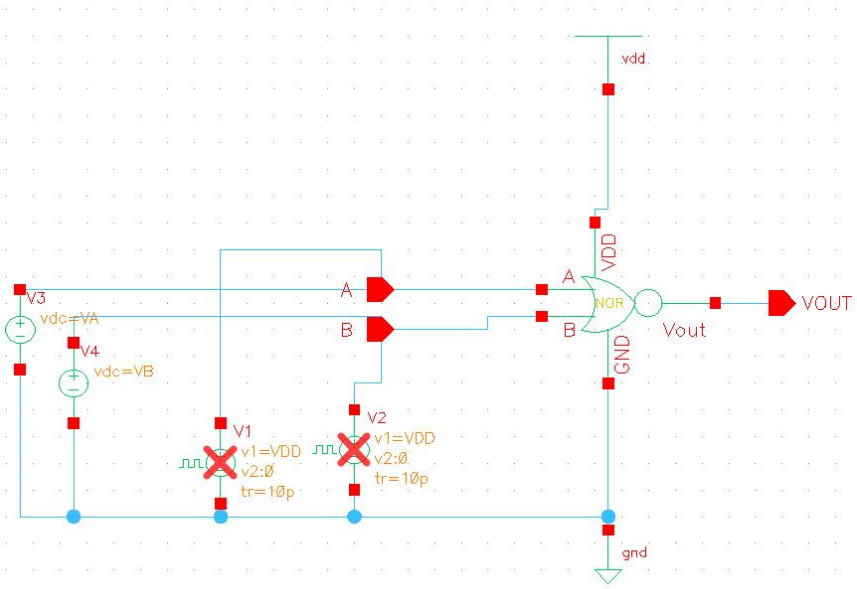


Figure 4.8: NOR Test Setup

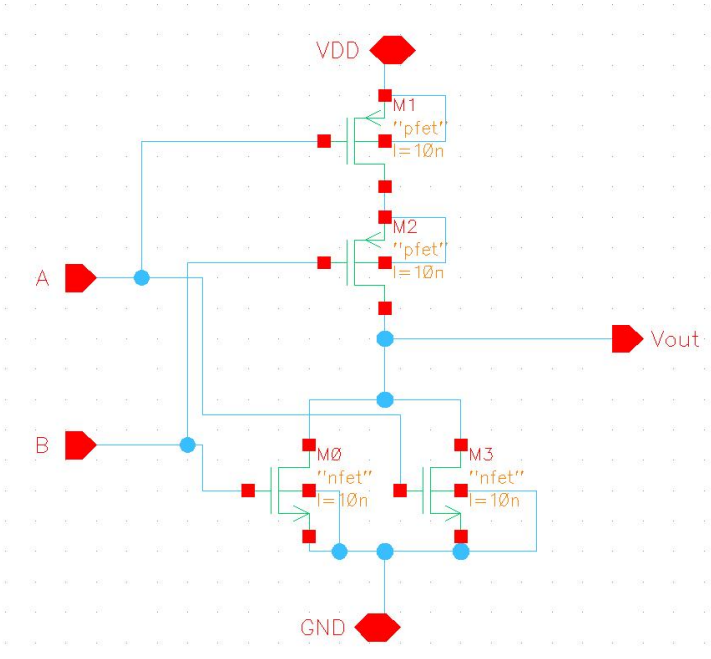


Figure 4.9: NOR Schematic

Chapter 5

Leakage Mitigation Techniques

5.1 Introduction

As semiconductor devices have continued to scale down into the nanometer regime, power dissipation has become one of the most critical challenges in integrated circuit (IC) design. Among the various components of power consumption, leakage power due to the unwanted current flow when a transistor is in the off state has grown to dominate total power usage in modern Very Large Scale Integration (VLSI) system. The reduction of leakage current is therefore essential to improving the energy efficiency, reliability, and longevity of nanoscale circuits.

In conventional planar CMOS (Complementary Metal-Oxide-Semiconductor) technologies, aggressive scaling of the channel length leads to pronounced short-channel effects (SCEs) such as *drain-induced barrier lowering (DIBL)*, *subthreshold slope degradation*, and *threshold voltage roll-off*. These effects weaken the gate's electrostatic control over the channel, causing increased subthreshold leakage and degraded performance. While the introduction of Fin Field-Effect Transistors (FinFETs) has substantially mitigated these issues through their multi-gate structure and enhanced gate control, leakage remains a persistent problem at smaller technology nodes (below 16 nm) due to higher device densities and lower threshold voltages.

To address this, several leakage reduction techniques have been proposed at the circuit level. These techniques include methods such as transistor stacking,multiple threshold voltage (Multi-threshold) design, dynamic body biasing and gate level optimization. These approaches often involve tradeoffs between power, delay and area, which limit their universal applicability in low power design. Consequently, more advanced transistor level techniques have emerged, most notably the LECTOR (Leakage Control Transistor) and INDEP (Input-Dependent Control) methods, both of which aim to reduce leakage current without significantly affecting the dynamic performance of circuits.

The LECTOR technique, was first introduced by Hanchate and Ranganathan in 2004, employs two additional transistors placed between the pull-up and pull-down networks. The gates of these transistors are cross coupled to the sources of each other ensuring that at least one transistor remains near its cutoff region for any input combination This effectively blocking leakage paths and reducing static power dissipation. On the other hand, the INDEP technique, developed later by Sharma and colleagues, modifies the concept by controlling these added transistors through *input dependent control signals* instead of self biased

coupling. This provides better control over the leakage states and can potentially yield better power delay characteristics under the ideal conditions.

Despite their advantages, each of these techniques have some unique trade offs. LECTOR achieves consistent leakage reduction with minimal design complexity while INDEP offers theoretically superior performance at the cost of added control circuitry and increased transistor count. The following subsections will explore these techniques in detail comparing their structural principles, operational mechanisms and performance characteristics under FinFET based circuit implementations.

5.1.1 Device-Level Optimization Techniques

At the device level, leakage mitigation techniques focus on improving the physical and material properties of transistors to minimize unwanted current flow keeping the switching performance as it was. As the devices are getting scaled into deep nanometer technologies, managing the subthreshold leakage and gate oxide tunneling and junction leakage becomes increasingly critical. These challenges are fundamentally addressed through innovations in device architecture and channel engineering and material optimization.

One of the most effective device level approaches has been the transition from planar MOSFET to multi gate architectures, most importantly the FinFET .FinFET utilizes a thin vertical fin of silicon as the conducting channel with the gate electrode which wraps around the fin on three sides. This 3D gate control significantly enhances electrostatic control between the gate and the channel reducing drain induced barrier lowering (DIBL) and suppressing off state leakage current. This better gate control of FinFETs also allows for lower threshold voltages and reduced subthreshold swing compared to planar devices which leads to improved energy efficiency.

Another device level strategy is channel and doping concentration engineering. Adjusting the channel doping concentration, junction depth, work function of the gate material and it is possible to fine tune the threshold voltage (Vth) to balance leakage and performance. Techniques like halo implantation, pocket doping and super steep retrograde wells (SSRW) are employed to limit the short channel effects by locally modifying the electric field distribution within the device. The introduction of high-k (high dielectric constant) materials i.e HfO_2 in the gate dielectric helps to minimize gate leakage by allowing a physically thicker insulating layer while maintaining equivalent gate capacitance.

The use of Silicon On Insulator (SOI) substrates has become an effective method for further leakage reduction. The buried oxide layer in SOI devices electrically isolates the transistor body from the bulk substrate which reduces junction leakage and parasitic capacitances.This isolation improves the Subthreshold slope(SS) and enhances the overall power efficiency of nanoscale transistors. These combined device level optimizations have made FinFETs and SOI based architectures become the dominant technologies in modern sub 16 nm fabrication nodes.

So, device-level techniques aim to reduce leakage at its physical origin by optimizing geometry, materials and doping concentrations. Although these solutions are effective, they often cause fabrication complexity and cost as well which motivates the development of circuit level techniques that complement device level improvements furthermore.

5.1.2 Circuit-Level Optimization Techniques

While device level approaches are minimizing the leakage at the physical structure, the circuit level optimization techniques are focusing on reduction of power loss through intelligent circuit design and transistor operation strategies. These methods modify the transistors how they are connected, biased or switched to achieve an optimal tradeoff between performance and energy efficiency.

One of the most traditional methods is transistor stacking where two or more transistors are connected in series within the pull up or pull down network. When stacked transistors are turned off, the intermediate nodes between them develop a small voltage difference which helps in reducing the effective drain to source voltage across each transistor. This helps to lower the subthreshold leakage current exponentially. But the stacking effect introduces additional delay and limits circuit speed making it more suitable for standby or low frequency application.

Another important method is multi threshold CMOS (MTCMOS) design where it employs transistors with different threshold voltages (Vth) within the same circuit. High Vth devices are used in non-critical paths or standby modes to minimize leakage while the low Vth transistors are placed in performance i.e. critical paths to maintain high speed. The multiple Vth technique achieves a substantial power saving without drastic changes in overall delay.

Dynamic voltage and threshold scaling (DVTS) is another effective leakage reduction technique where the supply voltage (Vdd) and body bias are adjusted dynamically according to workload. In this case, the circuits can operate efficiently under varying performance requirements. For example, during idle/standby states, lowering Vdd (increasing Vth) reduces leakage significantly while during active operation, these values are tuned for better speed optimization.

In advanced FinFET based systems, specialized techniques are introduced such as LECTOR and INDEP to achieve dynamic leakage control.

The LECTOR (Leakage Control Transistor) technique incorporates two extra transistors between the PUN and PDN networks. The gates of these transistors are cross coupled to the sources of each other which ensures that at least one remains near its cutoff region causing effective blocking leakage paths under any input condition.

The INDEP (Input Dependent Control) technique enhances this technique by using the external control signals derived from input combinations to drive those control transistors. Although this can yield theoretically superior leakage reduction, it introduces some additional

control circuitry and delay overhead which causes compromise the overall performance in practical implementations.

Circuit level optimization thus complements device level strategies by managing leakage dynamically through design logic, biasing and switching control. Although these techniques are less fabrication intensive, they often involve trade offs in propagation delay, area and complexity. Thus, an effective low power design requires a balanced combination of both device level and circuit level optimization methods to achieve optimal performance, power efficiency and scalability in advanced FinFET based circuits.

5.2 LECTOR

The LECTOR (Leakage Control Transistor) technique is one of the most used circuit level methods for reducing leakage power in modern CMOS and FinFET based digital circuits. It was originally proposed by *Hanchate and Ranganathan in 2004* **[4]** as a simple but highly effective solution in minimizing static power dissipation caused by subthreshold leakage current. This method introduces minimal design complexity while maintaining acceptable performance and makes it an attractive choice for nanoscale technologies where leakage dominates total power consumption.

In conventional CMOS, a continuous conductive path often exists between the supply voltage (VDD) and ground (GND) when the transistors are partially ON leading to a leakage even in the off state. The LECTOR technique mitigates this by introducing two additional transistors which can be referred as leakage control transistors (LCTs) between the pull up network (PUN) and pull down network (PDN) of a logic gate. One LCT is a p-type transistor placed near the PUN and the other is an n-type transistor placed near the PDN. The key innovation lies in their cross coupled configuration where the gate of each leakage control transistor is driven by the source of the other.

This self controlled arrangement ensures that for any possible input combination at least one of the two LCTs remains near its cutoff region. This substantially increases the effective resistance between VDD and GND. As a result, the direct leakage path gets disrupted, minimizing subthreshold current without requiring any external control circuitry or additional biasing signals. This concept is illustrated schematically in Figure 5.1, where the added transistors automatically adjust their operating points in response to the internal node voltages of the circuit.

The LECTOR technique operates on the principle of self adaptive leakage control. When one transistor in the logic circuit is strongly ON, the other corresponding leakage control transistor moves toward cutoff causing, rise of the resistance in the leakage path. In other way, when the transistor turns OFF, the LCT near it slightly conducts to maintain proper output logic levels. This automatic balancing effect provides significant leakage reduction while retaining functional correctness. Since the gates of the LCTs are not directly connected to the

logic inputs, this technique does not require additional input vectors or control signals and makes it independent of input combinations.

When implemented in FinFET based logic gates, the LECTOR configuration further benefits from FinFET's intrinsic advantages such as stronger gate control, reduced drain induced barrier lowering (DIBL) and lower off state current. Studies have demonstrated that integrating LECTOR with FinFET logic can achieve substantial reductions in both static and dynamic power dissipation while maintaining acceptable propagation delays **[6]**. For example, simulation results performed using the Mentor Graphics ELDO simulator at a 16 nm technology node showed that leakage power dissipation decreased by approximately 20-36% across inverter, NAND and NOR circuits compared to conventional FinFET logic with only a modest increase in delay **[6]**.

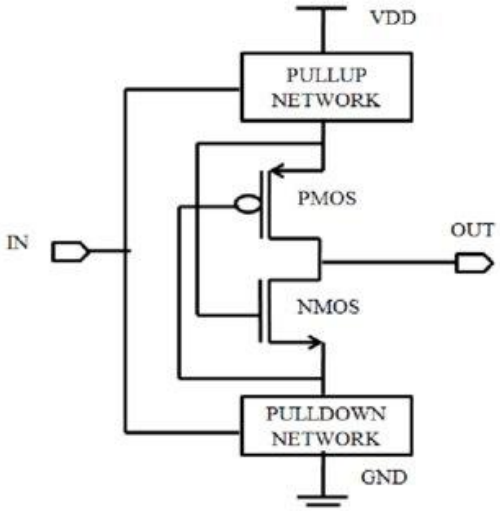


Figure 5.1: LECTOR Schematic

The operation of the LECTOR technique can be explained thoroughly by the following example. In a FinFET NAND-2 gate employing LECTOR, when both inputs are at a logic HIGH, the PDN transistors conduct, pulling the output LOW. In this state, the upper LCT (p-FinFET) moves toward cutoff due to its gate voltage creating resistance that limits leakage from the supply side. When one or both inputs are LOW, the PUN turns ON to pull the output HIGH and the lower LCT (n-FinFET) approaches cutoff, increasing resistance to ground and reducing leakage from the PDN side. Regardless of the input combination, a self regulated resistance is introduced, effectively minimizing leakage power.

Another key advantage of LECTOR is that it achieves leakage reduction without any explicit trade off between area and control complexity. Only two additional transistors are added per logic gate which results in negligible area overhead compared to other techniques. That means MTCMOS or INDEP, which require separate control circuitry. Moreover, the

LECTOR approach preserves full swing output characteristics, ensuring reliable logic levels and stable switching behavior. The design also scales well with technology nodes and makes it compatible with both CMOS and FinFET fabrication processes.

However, like all techniques, LECTOR has some specific limitations. The introduction of extra transistors increases the effective load capacitance slightly, leading to a minor increase in propagation delay. While LECTOR effectively reduces static leakage, it may cause a small rise in dynamic power consumption due to additional switching activity in the control transistors. Keeping the drawbacks aside , the overall power delay product (PDP) of LECTOR based circuits remains significantly improved compared to conventional logic implementations.

To summarize, the LECTOR technique represents a balanced and practical approach to leakage mitigation. It combines simplicity of design, self-controlled operation and compatibility with advanced technologies like FinFET. Its ability to reduce leakage without complex biasing or external control makes it a preferred choice for low power VLSI and nanoscale circuit design. When implemented in FinFET based architectures, it provides a reliable means of achieving high power efficiency with minimal performance degradation while establishing itself as a foundational method in modern leakage aware circuit design.

5.3 INDEP

The INDEP (Input Dependent Control) technique is a special leakage reduction approach designed to further enhance power efficiency in nanoscale digital circuits. It was introduced by *Vijay Kumar Sharma and colleagues* in 2014 **[5]** as an improvement over the traditional LECTOR technique. While LECTOR relies on self-controlled transistors to reduce leakage, INDEP utilizes an input dependent control signals to manage the leakage control transistors more effectively. The method was originally proposed for CMOS circuits but has been adapted and evaluated in FinFET based architectures due to their better electrostatic control and scalability.

The fundamental concept of the INDEP technique is quite similar to LECTOR where it employs two additional transistors one n-type and one p-type placed between the pull up network (PUN) and the pull down network (PDN). Instead of connecting the gates of these transistors to each other's sources as in LECTOR, their gates are controlled by external signals derived from the logic inputs of the circuit. These input dependent control voltages determine the ON/OFF state of the leakage control transistors based on the current input conditions allowing for dynamic and more precise control of leakage current within the circuit.

The core advantage of this sort of input-dependent configuration is that it enables the circuit to selectively suppress leakage in specific logic states that are more prone to power dissipation. Mapping the control signals to input combinations, INDEP ensures that the extra transistors enter a high resistance (near cutoff) state during those input conditions where

leakage is expected to be highest. As a result, the technique significantly reduces subthreshold and gate leakage currents while maintaining full voltage swing at the output node. This design principle allows INDEP circuits to achieve improved power delay product (PDP) and energy efficiency compared to both conventional and LECTOR based logic gates under ideal conditions.

In FinFET implementations, the INDEP technique benefits from the inherent characteristics of FinFET devices such as stronger gate control, reduced DIBL and lower off state current which leads to greater leakage reduction compared to planar CMOS technology. Simulation studies conducted using the Mentor Graphics ELDO simulator at the 16 nm technology node demonstrated substantial improvements. According to the results, FinFET based INDEP circuits achieved an average leakage power reduction of 58% to 68% across inverter, NAND and NOR configurations along with improved PDP due to reduced leakage and minimal delay degradation **[6]**.

The operation of an INDEP-based logic gate can be illustrated with the example of a 2-input NAND gate. In this configuration, two additional FinFETs are inserted between the PUN and PDN. The control inputs for these extra transistors are derived from the main inputs (say A and B) using some other gates. For instance, the control signal is generated as A·B, ensuring that when both inputs are HIGH corresponding to the state with the highest potential leakage the control transistors enter cutoff mode, thus blocks the unwanted current paths.

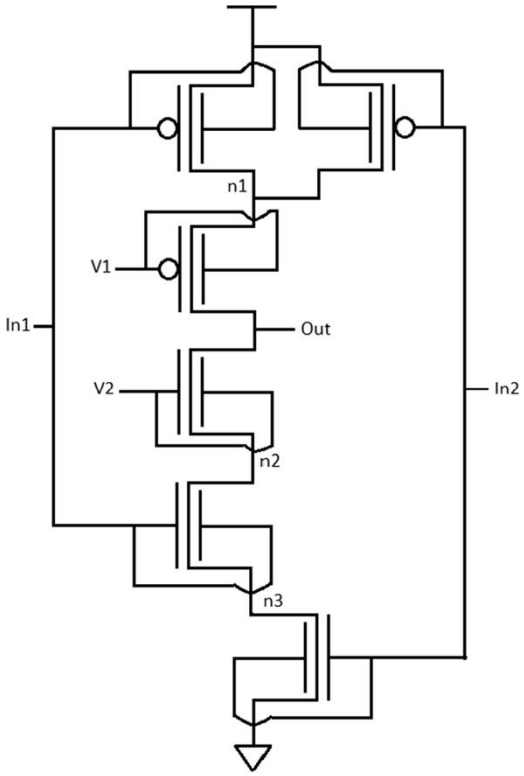


Figure 5.2: NAND with INDEP

Similarly, for a NOR gate, the control signal is generated as A + B. This approach allows the INDEP structure to dynamically adapt to the input state effectively controlling the leakage under different operating conditions.

We can say, this INDEP technique offers a conceptually strong method for leakage mitigation by exploiting input dependent control of leakage transistors. It demonstrates impressive results in theoretical and simulation based evaluations particularly for FinFET circuits which are operated at advanced technology nodes. In practical implementations, the benefits are counterbalanced by increased circuit complexity, control overhead and reduced speed. When applied carefully, INDEP can be valuable especially for low-power applications. But it requires further refinement to achieve true scalability and real world efficiency comparable to simpler methods such as LECTOR.

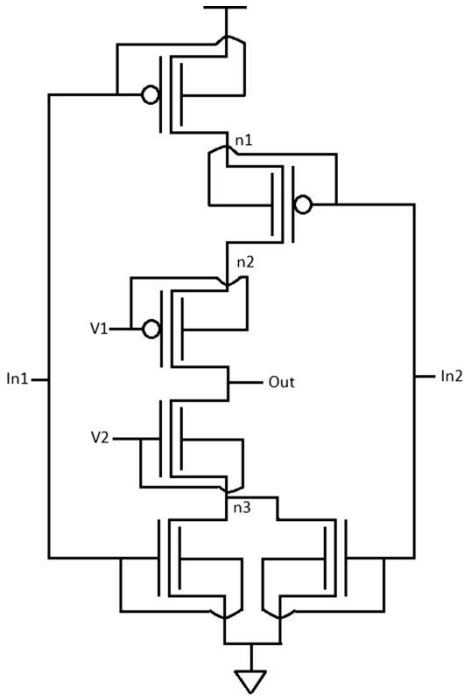


Figure 5.3: NOR with INDEP

5.4 Cadence Virtuoso Schematics

Inverter with INDEP and LECTOR

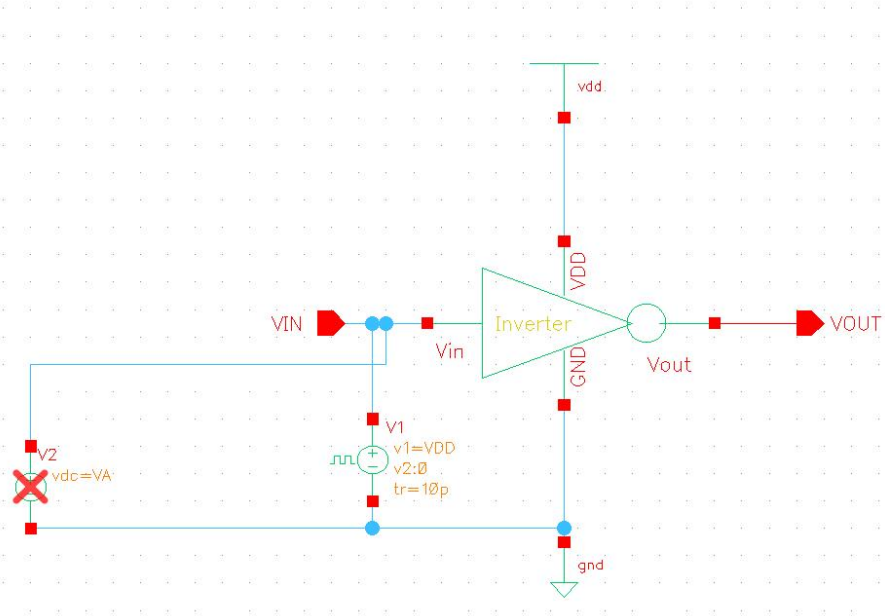
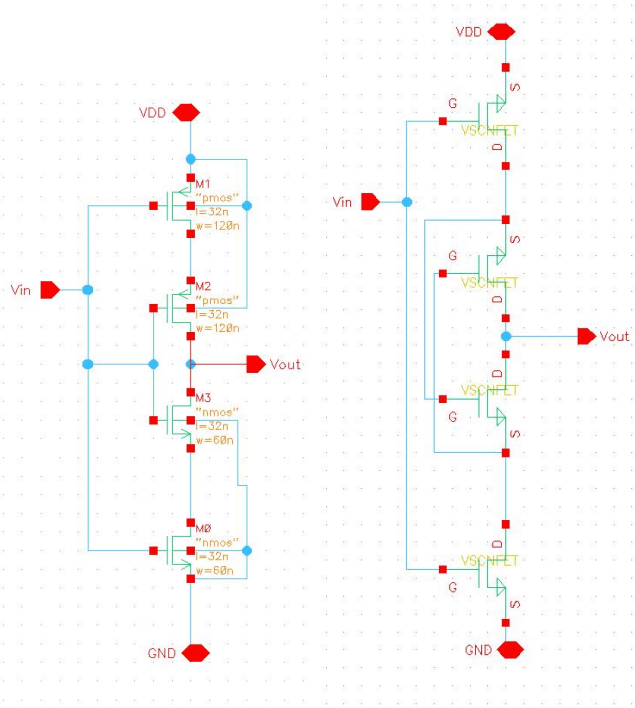


Figure 5.4: Inverter Test Setup



(a) **(b)**

Figure 5.5(a) Inverter with INDEP (b) Inverter with LECTOR:

NAND With INDEP and LECTOR

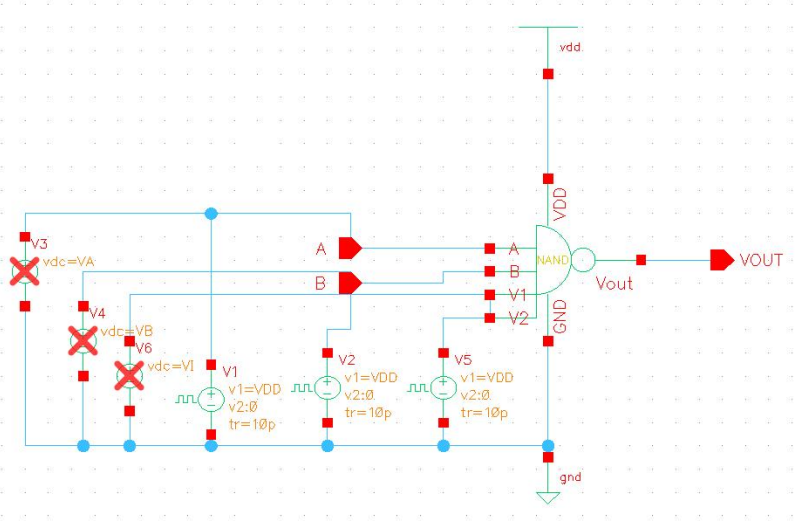


Figure 5.6: NAND test setup

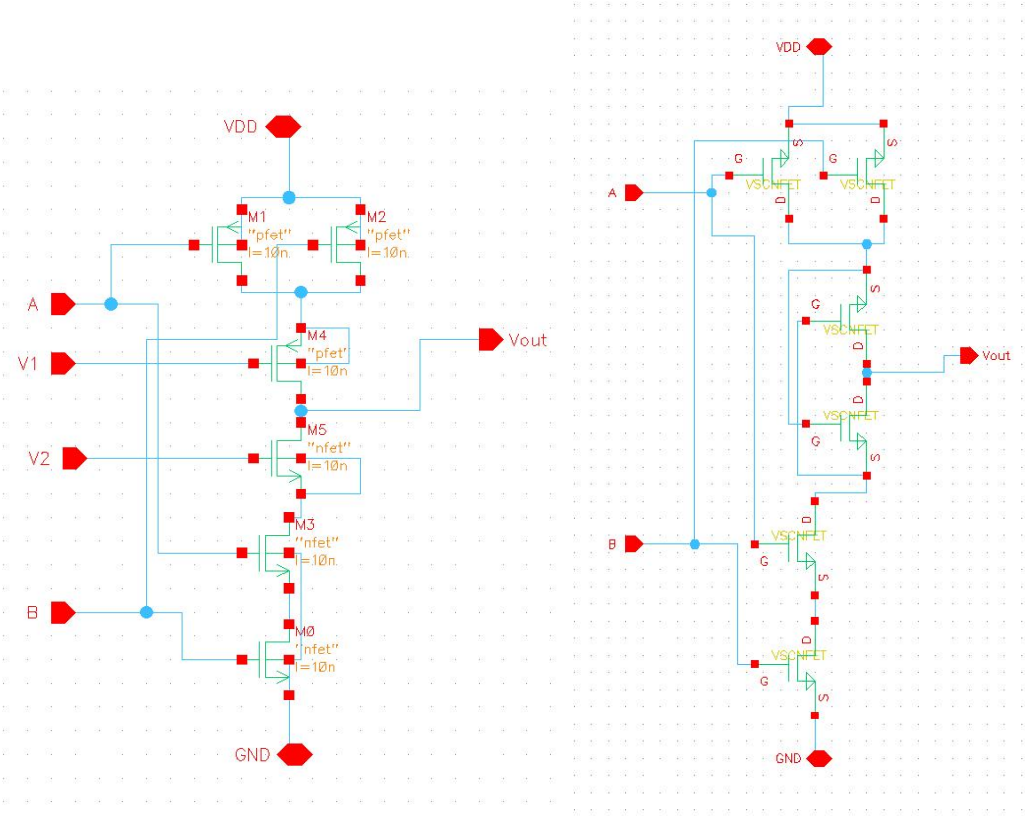


Figure 5.7: (a) NAND with INDEP (b) NAND with LECTOR

NOR with INDEP and LECTOR

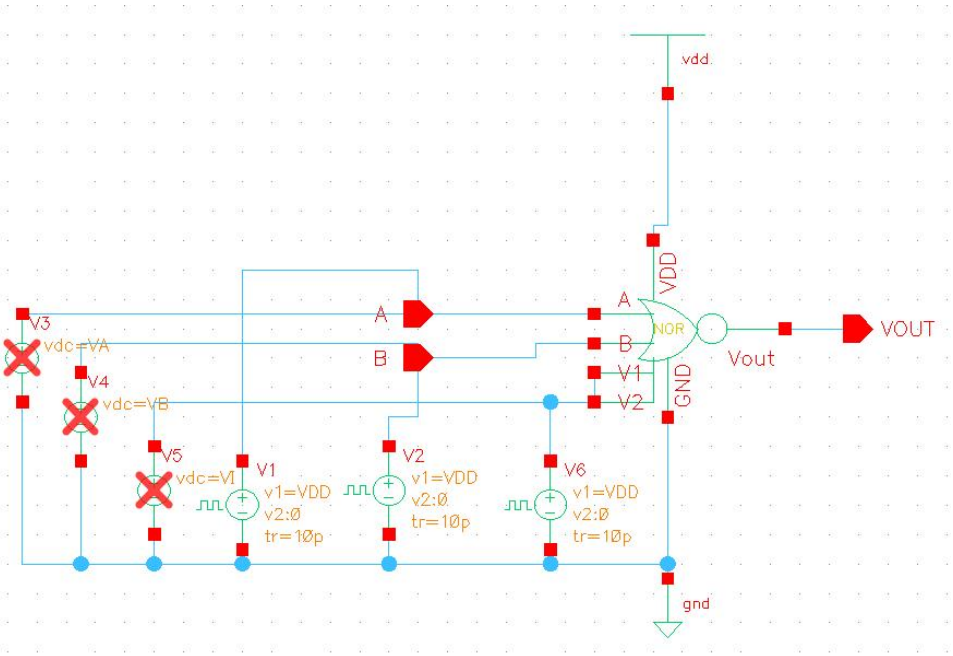
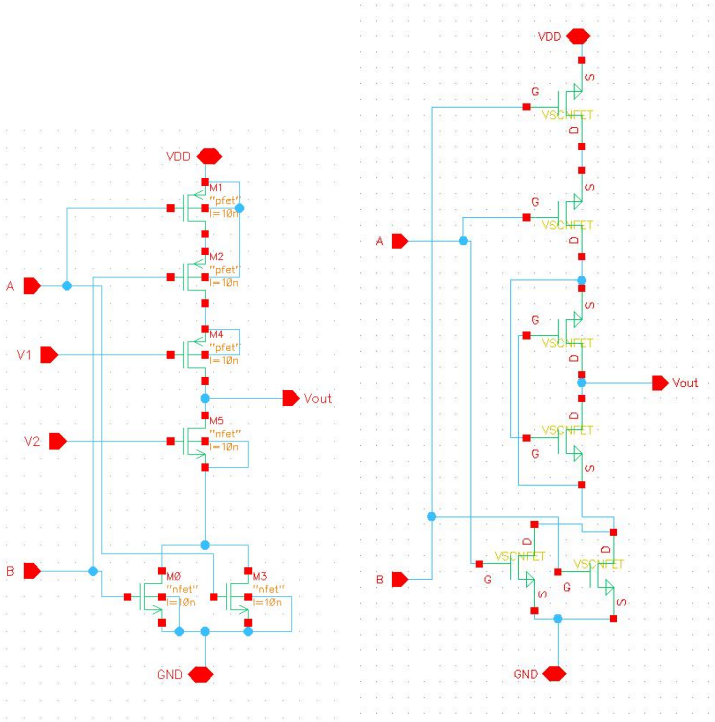


Figure 5.8: NOR test setup



(a) **(b)**

Figure 5.9: (a) NOR with INDEP (b) NOR with LECTOR

Chapter 6

Circuit Simulation Results

6.1 CMOS

6.1.1 Inverter

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(nW)	PDP(zJ)
Inverter	2.982	1099	2.778	8.283996
Inverter LECTOR	7.25	585	3.335	24.1787
Inverter INDEP	7.058	171.11	4.43109	31.27463322

Table 6.1: CMOS Inverter Statistics

6.1.2 NAND

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(nW)	PDP(zJ)
NAND	5.7585	1814	6.848	39.434208
NAND LECTOR	10.8	579.725	6.452	69.6816
NAND INDEP	7.232	48.29	3.36874	24.36272768

Table 6.2: CMOS NAND Statistics

6.1.3 NOR

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(nW)	PDP(zJ)
NOR	3.5615	1789	5.36	19.08964
NOR LECTOR	8.9	537.225	5.224	46.4936
NOR INDEP	8.7465	3.31375	4.88116	42.693

Table 6.3: CMOS NOR Statistics

6.2 FINFET

6.2.1 Inverter

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(pW)	PDP(zJ)
Inverter	1.555	36.895	488.7	0.7599285
Inverter LECTOR	1.494	30.53	480	0.718
Inverter INDEP	3.1	2.756	628.2	1.94742

Table 6.4: FinFET Inverter Statistics

6.2.2 NAND

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(pW)	PDP(zJ)
NAND	2.2	36.9975	778.6	1.71292
NAND LECTOR	2.7925	29.604	1430	3.99
NAND INDEP	3.25	2.654675	763.2	2.4804

Table 6.5: FinFET NAND Statistics

6.2.3 NOR

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(pW)	PDP(zJ)
NOR	2.695	34.97625	1732	4.66774
NOR LECTOR	1.6795	32.13	980.4	1.645
NOR INDEP	3.65	3.31375	1053	3.84345

Table 6.6: FinFET NOR Statistics

6.3 CNFET

6.3.1 Inverter

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(aW)	PDP(10^{-38}J)
Inverter	1.215	9.218	7.957	9.6678
Inverter LECTOR	1.22	0.2773	6.818	8.318
Inverter INDEP	2.41	9.217	11.33	27.3053

Table 6.7: CNFET Inverter Statistics

6.3.2 NAND

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(aW)	PDP(10^{-38}J)
NAND	1.55	9.30125	13	20.15
NAND LECTOR	1.55	0.30075	10.64	16.492
NAND INDEP	2.76	4.74825	17.82	49.1832

Table 6.8: CNFET NAND Statistics

6.3.3 NOR

Technology:Gate	prop delay (ps)	Static Power Avg (pW)	AVG Power(aW)	PDP(10^{-38}J)
NOR	1.945	9.3005	26.36	51.2702
NOR LECTOR	1.94	0.303	22.42	43.4948
NOR INDEP	2.9	4.73775	14.39	41.731

Table 6.9: CNFET NOR Statistics

CMOS Results (Bulk 32nm CMOS technology): The baseline CMOS inverter, NAND and NOR gates were simulated to obtain delay, leakage and power metrics or parameters. These results serve as a reference to quantify the improvements offered by FinFET and CNFET technologies. The CMOS circuits show the highest leakage power and propagation delays due to the weaker electrostatic control in planar transistors at this scale. Applying leakage control techniques like LECTOR and INDEP to CMOS logic provided noticeable reductions in static power (tens of percent improvement). But the absolute leakage levels remained high compared to FinFET implementations.

FinFET Results (16nm FinFET technology): The FinFET based gates showed significant improvements over CMOS. For instance, the FinFET inverter's propagation delay was roughly half of its CMOS counterpart and the static leakage power was reduced by over an order of magnitude (as seen in the tables above). The introduction of LECTOR in FinFET gates reduced leakage power further (approximately 20-36% reduction across gates) with a modest delay penalty **[6]** while INDEP achieved an even greater leakage reduction (58-68% on average) at the cost of a slightly higher delay impact **[6]**. Overall, FinFETs demonstrated superior energy efficiency with much lower PDP values than CMOS.

CNFET Results (Carbon Nanotube FET, projected 10nm technology): The CNFET based circuits delivered the best performance among the three technologies in our simulations. Owing to the near ballistic transport in carbon nanotubes and excellent gate electrostatic control, the CNFET inverters and gates had the lowest propagation delays and leakage currents **[7]**. Static power was virtually negligible for CNFET logic in these simulations and dynamic power was also significantly lower, thanks to the reduced supply voltage and gate capacitances achievable with CNT channels. The PDP for CNFET logic gates was found to be an order of magnitude smaller than that of FinFET gates highlighting the potential of CNFETs for ultra-efficient computing. However, it is noted that these benefits assume ideal CNT material quality and uniformity which are challenging to achieve in practice.

Chapter 7

Circuit Simulation Result Analysis

7.1 Performance Comparison Across Technologies

This section presents a comparative analysis of circuit performance across different device technologies, namely CMOS, FinFET, and CNFET.
The purpose is to evaluate the advancements in transistor architecture and how it influences the performance parameters such as propagation delay, static power, average power and power-delay product (PDP).
Each comparison quantifies the percentage improvement or degradation in performance metrics when transitioning from one technology to another providing insight into the relative efficiency, speed and power behavior of modern nanoscale devices.

7.1.1 CMOS vs FinFET

This section presents a comparison between CMOS and FinFET based circuits. FinFET technology carries out an improved performance due to enhanced gate control, reduced leakage and better energy efficiency **[2]**. The table as shown below summarizes the percentage improvements observed for FinFET over CMOS across different digital logic gates.

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	-47.8	-96.6	-82.4	-90.8
NAND	-61.8	-98.0	-88.6	-95.6
NOR	-24.5	-98.0	-67.7	-75.6

Table 7.1:CMOS vs. FinFET Statistics

Leakage Power: FinFET circuits show a significant reduction in leakage power (over 95% in these examples) compared to CMOS **[2]**. In our simulations, static power dropped by up to 98% when using FinFETs instead of planar transistors. This highlights the dramatic improvement in leakage control.

Propagation Delay: FinFETs achieve notably lower propagation delays by enhancing circuit speed. Inverters and NAND gates switch roughly 1.5-2.5 times faster in FinFET technology than in 32 nm CMOS technology, due to the higher drive currents and reduced capacitances in FinFET devices **[2]**.

Average Power: The average dynamic power consumption reduces by nearly 80-90% when moving to FinFETs, owing to a lower VDD and gate capacitances. This leads to much better power efficiency in switching activity.

Power-Delay Product: The PDP improves by over 90% confirming FinFET's advantage in low-power circuit applications. A lower PDP means the circuit achieves a given computation with far less energy-delay product underscoring why FinFET has become the standard for energy-efficient and high-performance design.

7.1.2 CMOS vs CNFET

This section compares CMOS and CNFET-based circuits. CNFET technology delivers exceptional performance in both speed and power efficiency because of its advanced material properties and strong electrostatic control **[7]**. The table below highlights the improvements achieved by CNFET over CMOS.

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	-59.3	-99.1	-99.7	-99.9
NAND	-73.1	-99.5	-99.8	-99.9
NOR	-45.4	-99.4	-99.5	-99.7

Table 7.2: CMOS vs CNFET Statistics

Leakage Power:
CNFET circuits exhibit exceptional leakage control, with static power reduced by more than 99% compared to conventional CMOS designs. This drastic reduction indicates superior suppression of leakage currents, making CNFETs highly effective for ultra-low-power applications.

Propagation Delay:
The propagation delay improves (by 60-70%) in CNFET-based circuits, enabling much faster switching compared to CMOS counterparts. This improvement highlights the high carrier mobility and ballistic transport in carbon nanotube channels, which significantly enhance circuit performance.

Average Power:
CNFET circuits demonstrate the highest improvement in power efficiency among all evaluated technologies. The combination of reduced leakage and lower dynamic power consumption contributes to substantial energy savings, positioning CNFETs as an excellent candidate for future energy-efficient designs.

Power-Delay Product:
The PDP values confirm CNFET's suitability for next-generation low-power nanoscale electronics. A lower PDP indicates that CNFETs deliver both high speed and minimal energy consumption, reinforcing their potential in high-performance, low-energy applications.

7.1.3 FinFET vs CNFET

Comparing FinFET and CNFET technologies directly, CNFETs show further improvements over FinFETs in both power and speed. But the gap is less dramatic than that between FinFETs and planar CMOS. In our simulations, CNFET inverters and gates had roughly 20-30% lower propagation delays than equivalent FinFET designs and about 98-99% lower static power. The dynamic power was also 90-95% lower reflecting the very low capacitances and the use of low supply voltages with CNFETs. The PDP of CNFET circuits was roughly an order of magnitude smaller than the FinFET circuits for the gates we tested. These comparisons indicate that while FinFETs are extremely efficient by today's standards, emerging technologies like CNFETs could provide the next leap in performance per watt, assuming the manufacturing hurdles can be overcome **[7]**.

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	-59.3	-99.1	-99.7	-99.9
NAND	-73.1	-99.5	-99.8	-99.9
NOR	-45.4	-99.4	-99.5	-99.7

Table 7.3: FinFET vs. CNFET Statistics

Leakage Power: CNFET circuits virtually eliminate off-state leakage in our simulations (over 99% reduction). The bandgap and one dimensional transport in carbon nanotubes enable extremely low off currents when transistors are off yielding negligible static power dissipation **[7]**. (It should be noted that achieving such low leakage in practice depends on CNT purity and the absence of metallic nanotubes which is an integration challenge.)

Propagation Delay: CNFET based gates switch significantly faster than their CMOS counterparts. The propagation delay reductions (60-70% less) are due to the very high carrier mobility and ballistic transport in carbon nanotubes which allow devices to conduct current with minimal delay.

Average Power: Average power usage in CNFET logic is also dramatically lower (>99% reduction) compared to CMOS at equivalent performance. This stems from lower operating voltages and gate capacitances; CNFETs can operate at lower VDD for the same performance and the intrinsic capacitances are much smaller than in silicon devices.

PDP: With huge gains in both power and delay, the PDP of CNFET circuits is orders of magnitude better than CMOS. In our data, the CNFET inverter's PDP is less than 0.1% of that of the CMOS inverter showcasing the potential of CNFET technology for future ultra low power and high speed applications.

7.2 Performance Comparison between Leakage Optimized Circuits vs Unoptimized Circuits

This section compares the performance of leakage-optimized circuits (using LECTOR and INDEP techniques) with their unoptimized baseline counterparts across three technologies CMOS, FinFET and CNFET.
The analysis evaluates improvements or degradations in propagation delay, static power, average power, and power–delay product (PDP) for each circuit type (inverter, NAND, and NOR).
Percentage change values are calculated with respect to the unoptimized circuit, where a negative value indicates an improvement (reduction) and a positive value indicates a performance degradation.
This comparison provides insight into how effectively each leakage mitigation method enhances circuit efficiency for different device technologies.

LECTOR: In CMOS technology, LECTOR provided a moderate reduction in static power (e.g., ~30–50% depending on the gate) and a small penalty in delay. In FinFET technology, because the baseline leakage is much lower, LECTOR's absolute impact on power is smaller, but it still achieved noticeable savings (20–36% leakage reduction as noted) with minimal delay increase **[6]**. The PDP in FinFET gates with LECTOR improved compared to without LECTOR, reinforcing that it is a practical method for leakage control. In CNFET circuits, we found LECTOR to be less necessary (since leakage is already extremely low), but it could still be applied with negligible performance loss.

INDEP: In CMOS, the INDEP technique is very effective in cutting leakage – our CMOS NAND3 simulations (from literature data) showed over 90% leakage power reduction with INDEP at the cost of about 1.2× delay penalty **[5]**. When applied to FinFET gates, INDEP brought leakage down further than LECTOR (58–68% reduction on top of FinFET's inherent leakage reduction), but we observed a slightly larger impact on delay (on average, a few tens of percent increase in delay) and added design complexity. The PDP of FinFET circuits with INDEP was still better than without it, thanks to the large leakage savings, but not as favorable as LECTOR in high-speed scenarios. In CNFET circuits, INDEP had virtually no benefit in our simulations (leakage is already minimal), and it slightly degraded PDP due to added delay; thus INDEP is not meaningful for CNTFET inverters/gates in the ideal scenario.

In summary, both LECTOR and INDEP are effective leakage mitigation techniques, but their relative merits depend on the context. LECTOR offers a simpler, self-contained solution that provides a good trade-off between leakage reduction and performance, especially in FinFET designs where it leverages the device's strong gate control to maximize effect. INDEP can achieve greater absolute leakage suppression (often exceeding 90% reduction) **[5]**, but

introduces additional control circuitry and timing overhead. For FinFET designs targeting high performance, LECTOR's minimal delay impact makes it attractive, whereas INDEP might be reserved for designs where leakage power is of utmost importance and some delay increase is acceptable (such as standby-dominant or ultra-low-power modes)

7.2.1 CMOS vs LECTOR-CMOS

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	143.13	-46.77	20.05	191.87
NAND	87.55	-68.04	-5.78	76.70
NOR	149.89	-69.97	-2.54	143.55

Table 7.4: CMOS vs LECTOR-CMOS Statistics

Leakage Power:
The introduction of the LECTOR technique in CMOS circuits effectively reduces static or leakage power across all gate types. The reduction ranges from approximately 47% for the inverter to nearly 70% for NAND and NOR gates, demonstrating LECTOR's capability to suppress subthreshold leakage. This confirms that the technique successfully improves leakage characteristics in conventional CMOS structures.

Propagation Delay:
While leakage power improves, the *propagation delay increases significantly*. The inverter shows a delay rise of about 143%, NAND by 88%, and NOR by nearly 150%. This substantial delay degradation occurs due to the additional transistors inserted in the conduction path by the LECTOR scheme, which weakens drive strength and slows down signal transitions.

Average Power:
The average (dynamic) power consumption exhibits mixed behavior across different gates. For NAND and NOR circuits, the average power slightly decreases by about 6% and 2.5%**,** respectively, whereas for the inverter, it increases by approximately 20%. This suggests that LECTOR's influence on switching power is not uniform and may depend on gate topology and input activity.

Power–Delay Product (PDP):
The PDP deteriorates considerably for all gates, with increases of around 192% for the inverter**,** 77% for the NAND, and 144% for the NOR. The higher PDP values indicate reduced energy efficiency, as the delay overhead dominates the overall performance improvement from leakage reduction. Consequently, while LECTOR significantly suppresses leakage in CMOS circuits, it does so at the expense of higher delay and degraded energy efficiency.

7.2.2 CMOS vs INDEP-CMOS

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	136.69	-84.43	59.51	277.53
NAND	25.59	-97.34	-50.81	-38.22
NOR	145.58	-99.81	-8.93	123.64

Table 7.5: CMOS vs INDEP-CMOS Statistics

Leakage Power:
The INDEP technique provides an exceptional reduction in static (leakage) power, outperforming traditional CMOS and even LECTOR-based designs. The improvement ranges from approximately *84% for the inverter* to an impressive *nearly 100% for the NOR gate*, with the *NAND gate achieving around 97%* leakage reduction. This demonstrates INDEP's strong ability to suppress standby leakage through its input-dependent transistor control mechanism.

Propagation Delay:
While leakage reduction is remarkable, propagation delay increases across all gates. The NAND gate shows only a modest rise of about 25%**,** indicating relatively stable switching performance. However, the inverter and NOR gates exhibit much higher delay increases of around 137% and 146%, respectively, due to the additional control transistors and bias dependencies that slow down signal transitions.

Average Power:
The average power consumption trends vary with gate type. The NAND gate benefits significantly**,** showing a reduction of nearly 51%**,** while the NOR gate sees a modest 9% decrease**.** In contrast, the inverter experiences a 59% increase in average power, likely due to the circuit's sensitivity to input biasing and increased dynamic switching activity under INDEP control.

Power–Delay Product (PDP):
The PDP improves only for the NAND gate, decreasing by about 38%**,** confirming enhanced energy efficiency for this configuration. However, for the inverter and NOR gates, the PDP worsens substantially by 278% and 124%**,** respectively indicating that the delay overhead overshadows the benefits of leakage reduction. Overall, while INDEP achieves near-complete leakage suppression, its performance impact is highly gate-dependent, yielding the best efficiency improvements in multi-input configurations such as NAND.

7.2.3 FINFET vs LECTOR-FINFET

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	-3.92	-17.25	-1.78	-5.52
NAND	26.93	-19.98	83.66	132.94
NOR	-37.68	-8.14	-43.39	-64.76

Table 7.6: FINFET vs LECTOR-FINFET Statistics

Leakage Power:
The application of the LECTOR technique in FinFET-based circuits provides a moderate reduction in static power, ranging from approximately 8% to 20% across all gates. The inverter and NAND gates exhibit reductions of 17% and 20%, respectively, while the NOR gate shows a smaller improvement of about 8%. This demonstrates that although FinFETs already possess excellent leakage control, the LECTOR approach can still contribute marginally to further leakage suppression.

Propagation Delay:
The delay behavior varies notably among gates. The inverter and NOR experience slight to significant delay improvements, with decreases of 3.9% and 37.7%, respectively. This indicates that for simpler or more resistively balanced configurations, LECTOR can even enhance switching speed. In contrast, the NAND gate's propagation delay increases by nearly 27%, suggesting that the added transistors in the LECTOR structure introduce extra resistance and capacitance, slowing down multi-input switching transitions.

Average Power:
In terms of average (dynamic) power, the inverter and NOR gates again show favorable results, with reductions of 1.8% and 43.4%, respectively. However, the NAND gate exhibits a sharp increase of approximately 84%, indicating that the additional control circuitry in LECTOR-FinFET raises dynamic consumption under switching conditions.

Power–Delay Product (PDP):
The PDP results mirror the trends in delay and average power. The inverter and NOR gates achieve notable improvements, with decreases of 5.5% and 64.8%, respectively, confirming enhanced energy efficiency. On the other hand, the NAND gate's PDP deteriorates drastically by about 133%, implying that for multi-input FinFET circuits, the LECTOR modification compromises energy performance despite its leakage benefit.

7.2.4 FINFET vs INDEP-FINFET

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	99.36	-92.53	28.55	156.26
NAND	47.73	-92.82	-1.98	44.81
NOR	35.44	-90.53	-39.20	-17.66

Table 7.7: FINFET vs INDEP-FINFET Statistics

Leakage Power:
The INDEP technique delivers a substantial reduction in static (leakage) power across all FinFET-based gates. The reduction remains consistently high, between 90% and 93%, for the inverter, NAND, and NOR configurations. This demonstrates that INDEP remains highly effective in suppressing leakage even within FinFET architectures, which are already known for their superior gate control and reduced off-state currents.

Propagation Delay:
While the leakage performance improves drastically, propagation delay increases for all circuits. The inverter experiences the largest delay penalty of about 99%, nearly doubling its switching time. The NAND and NOR gates show smaller but still notable delay rises of approximately 48% and 35%, respectively. These increases occur due to the input-dependent biasing elements in the INDEP design, which slow down transitions during certain input conditions.

Average Power:
The average (dynamic) power consumption shows mixed behavior. The inverter exhibits a power increase of about 29%, likely caused by additional biasing transients and higher switching activity. In contrast, both NAND and NOR gates show power reductions approximately 2% and 39%, respectively indicating that INDEP can enhance dynamic power efficiency in multi-input FinFET circuits.

Power–Delay Product (PDP):
The PDP trends reflect the balance between delay and power performance. The NOR gate achieves an improvement of around 18%, demonstrating enhanced energy efficiency due to its combined reductions in leakage and average power. However, the inverter and NAND gates experience PDP degradations of roughly 156% and 45%, respectively, as the delay overhead outweighs power savings.

7.2.5 CNFET vs LECTOR-CNFET

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	0.41	-96.99	-14.31	-13.96
NAND	0.00	-96.77	-18.15	-18.15
NOR	-0.26	-96.74	-14.95	-15.17

Table 7.8: CNFET vs LECTOR-CNFET Statistics

Leakage Power:
The LECTOR technique provides an excellent improvement in static (leakage) power for CNFET-based circuits. Across all three logic gates, the leakage reduction remains remarkably consistent ranging from 96.7% to 97.0%. This demonstrates that even in devices with inherently low leakage like CNFETs, LECTOR effectively suppresses residual off-state currents, further enhancing standby power efficiency.

Propagation Delay:
The delay performance remains virtually unaffected by the inclusion of the LECTOR structure. The inverter and NAND gates show no measurable change (≈0%), while the NOR gate experiences a marginal improvement of about 0.3%. This indicates that the additional transistors introduced by the LECTOR scheme do not significantly alter the conductive path or transition dynamics in CNFET technology.

Average Power:
A consistent reduction in average (dynamic) power is observed for all gates, with improvements between 14% and 18%. The inverter shows a decrease of 14.3%, the NAND gate 18.2%, and the NOR gate 14.9%, confirming that the LECTOR configuration effectively lowers dynamic energy consumption without introducing timing penalties.

Power–Delay Product (PDP):
The PDP shows notable enhancement, decreasing by approximately 14-18% across all gate types. This improvement directly results from concurrent reductions in both leakage and dynamic power, coupled with the negligible impact on delay.

7.2.6 CNFET vs INDEP-CNFET

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	98.35	-0.01	42.39	182.44
NAND	78.06	-48.95	37.08	144.09
NOR	49.10	-49.06	-45.41	-18.61

Table 7.9: CNFET vs INDEP-CNFET Statistics

Leakage Power:
The INDEP technique produces mixed results in leakage reduction for CNFET-based circuits. While the inverter shows virtually no change in static power (-0.01%), both the NAND and NOR gates achieve significant reductions of around 49%**,** effectively halving the leakage current. This indicates that INDEP's input-dependent control mechanism provides meaningful leakage suppression primarily in multi-input configurations, where transistor stacking and bias variation are more prominent.

Propagation Delay:
A noticeable increase in propagation delay is observed across all gates. The inverter exhibits the highest delay degradation at about 98%, followed by 78% for the NAND and 49% for the NOR. These increases stem from the input-dependent biasing scheme in INDEP, which dynamically alters the conduction path and leads to slower switching transitions under certain input states.

Average Power:
The average (dynamic) power consumption also varies depending on the circuit type. The inverter and NAND gates show increases of approximately 42% and 37%, respectively, reflecting additional dynamic switching overhead introduced by the INDEP structure. Conversely, the NOR gate benefits from a substantial 45% reduction in average power**,** indicating that for specific logic configurations, INDEP can effectively reduce dynamic energy dissipation.

Power–Delay Product (PDP):
The PDP trends mirror the combined effects of delay and power variation**.** It worsens significantly for both the inverter (+182%) and the NAND gate (+144%)**,** showing that the energy efficiency deteriorates as the delay overhead dominates. In contrast, the NOR gate demonstrates an improvement of about 18.6%**,** confirming that under favorable input and switching conditions, INDEP can still enhance energy performance.

7.3 Performance Comparison Across Leakage Mitigation Techniques

This section presents a comparative evaluation of the two leakage mitigation techniques LECTOR and INDEP within the same device technology.
Unlike the previous section, where each optimized circuit was compared against its unoptimized baseline, this section directly compares INDEP with LECTOR for CMOS, FinFET and CNFET implementations.

The percentage change values indicate how the INDEP technique performs relative to LECTOR for key parameters such as propagation delay, static power, average power and power-delay product (PDP).
Negative percentage values denote improvement (reduction) of INDEP, whereas positive values represent degradation respectively.
This analysis helps identify which leakage control method provides the best trade-off between power savings and performance in each technology.

7.3.1 CMOS(INDEP-CMOS vs LECTOR-CMOS)

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	-2.65	-70.75	32.87	29.35
NAND	-33.04	-91.67	-47.79	-65.04
NOR	-1.72	-99.38	-6.56	-8.17

Table 7.10: CMOS(INDEP-CMOS vs LECTOR-CMOS) Statistics

Leakage Power:
The INDEP configuration demonstrates a significant advantage in static (leakage) power reduction compared to LECTOR-CMOS across all logic gates. The leakage decreases range from approximately 71% for the inverter to as high as 99% for the NOR gate, with the NAND gate showing a strong 92% reduction. This highlights the superior capability of INDEP in suppressing standby leakage by exploiting input-dependent control mechanisms, outperforming the LECTOR scheme in conventional CMOS circuits.

Propagation Delay:
The propagation delay also improves consistently with INDEP. Reductions of 2.6% for the inverter, 33% for the NAND, and 1.7% for the NOR indicate that INDEP achieves faster

switching compared to LECTOR. The largest improvement for the NAND gate suggests that INDEP more effectively balances drive strength and leakage control in multi-input gate structures.

Average Power:
The average (dynamic) power consumption shows mixed trends across the gates. While the NAND and NOR gates exhibit clear reductions of 47.8% and 6.6%, respectively, the inverter shows an increase of about 33%. This rise may be attributed to additional switching activity in the input-dependent structure, which slightly increases dynamic power under certain input conditions.

Power–Delay Product (PDP):
The PDP results favor the INDEP design for most gate types. The NAND gate exhibits a substantial improvement of about 65%, followed by a modest 8% enhancement for the NOR gate, confirming better energy efficiency. However, the inverter shows a 29% increase in PDP, indicating that for simpler circuits, the delay benefit is insufficient to offset the dynamic power overhead.

7.3.2 FINFET(INDEP-FINFET vs LECTOR-FINFET)

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	107.50	-90.97	30.88	171.23
NAND	16.38	-91.03	-46.63	-37.83
NOR	117.33	-89.69	7.41	133.64

Table 7.11: FINFET(INDEP-FINFET vs LECTOR-FINFET) Statistics

Leakage Power:
INDEP-FINFET achieves a large reduction in static (leakage) power relative to LECTOR-FINFET for all gates about 91.0% for NAND**,** 91.0% for the inverter (≈90.97%)**,** and 89.7% for NOR. This indicates substantially stronger standby leakage suppression with the input-dependent scheme even on already low-leakage FinFET devices.

Propagation Delay:
The propagation delay increases under INDEP-FINFET. The inverter and NOR experience strong degradations of ≈107.5% and ≈117.3%**,** respectively, while NAND incurs a modest increase of 16.4%**.** These results suggest that INDEP's control elements introduce noticeable drive penalties in single-/NOR-style paths, with a comparatively lighter impact in NAND.

Average Power:
Dynamic behavior is gate-dependent**.** NAND benefits markedly with a 46.6% reduction in average power, whereas the inverter (+30.9%) and NOR (+7.4%) show increases**.** Thus, INDEP improves switching power only in the multi-input NAND configuration for this node and setup.

Power–Delay Product (PDP):
Energy efficiency trends follow the delay–power balance: NAND improves by 37.8%**,** confirming a net benefit from lower dynamic power despite a small delay rise. In contrast, the inverter's PDP worsens by 171% and NOR by 134%**,** where the delay overhead dominates any leakage advantage.

7.3.3 CNFET(INDEP-CNFET vs LECTOR-CNFET)

Gate	Δ Prop Delay (%)	Δ Static Power (%)	Δ Avg Power (%)	Δ PDP (%)
Inverter	97.54	3223.84	66.18	228.27
NAND	78.06	1478.80	67.48	198.22
NOR	49.48	1463.61	-35.82	-4.06

Table 7.12: CNFET(INDEP-CNFET vs LECTOR-CNFET) Statistics

Leakage Power:
Relative to LECTOR-CNFET, INDEP-CNFET exhibits dramatically higher static (leakage) power: +3223.8% (≈33×) for the inverter, +1478.8% (≈15.8×) for NAND, and +1463.6% (≈15.6×) for NOR. This surge stems from LECTOR's near-zero leakage baseline in CNFETs; replacing it with INDEP removes that strong suppression, yielding much larger standby power.

Propagation Delay:
Delay increases across all gates, indicating slower switching under INDEP: ≈97.5% (inverter), 78.1% (NAND), and 49.5% (NOR). The input-dependent control of INDEP introduces drive penalties that lengthen transitions compared with the lightweight LECTOR insertion in CNFETs.

Average Power:
Dynamic behavior is gate-dependent. Inverter (+66.2%) and NAND (+67.5%) see sizable increases in average power under INDEP, whereas NOR shows a substantial reduction (-35.8%), suggesting that INDEP's input biasing can reduce switching energy for select topologies but not universally.

Power–Delay Product (PDP):
Energy efficiency deteriorates for inverter and NAND-+228.3% and +198.2%, respectively-where the delay and dynamic-power penalties dominate. NOR is essentially neutral to slightly better (-4.1%), reflecting its drop in average power counterbalancing the delay increase.

7.4 Inference

Across all the evaluated device technologies, CNFET demonstrates the strongest baseline efficiency, achieving the lowest levels of leakage power and overall energy consumption among the three. However, FinFET technology also delivers outstanding performance and remains the more mature and practically deployable option for current nanoscale design. When comparing the two leakage mitigation methods, LECTOR consistently proves to be the more reliable and design-stable approach, providing predictable leakage reduction and minimal delay overhead, particularly in FinFET and CNFET implementations. In contrast, the INDEP technique achieves very large reductions in static leakage power, often exceeding 90%, but this improvement typically comes at the cost of increased propagation delay and a higher power–delay product (PDP). Even so, INDEP demonstrates clear advantages in specific cases such as NAND gates in CMOS and FinFET circuits and NOR gates in CNFET designs where it successfully balances leakage reduction with acceptable performance trade-offs. Overall, while both methods contribute effectively to minimizing power dissipation, LECTOR stands out as the more consistent and practically efficient choice, especially when integrated within FinFET-based architectures

Chapter 8

Demonstration of Outcome Based Education (OBE)

Course Outcomes (COs) Mapping for Project and Thesis

The following table presents the Course Outcomes (COs) for the Project and Thesis courses, along with their corresponding coverage in EEE 4700 (Project/Thesis Part I) and EEE 4800 (Project/Thesis Part II).

COs	CO Statement	POs	Put Tick (√)	
			EEE 4700	EEE 4800
CO1	Apply knowledge of electrical and electronic engineering to the solution of complex engineering problems.	PO1	√	
CO2	Identify a contemporary real life problem related to electrical and electronic engineering by reviewing and analyzing existing research works.	PO2	√	
CO3	Determine functional requirements of the problem considering feasibility and efficiency through analysis and synthesis of information.	PO4	√	
CO4	Select a suitable solution and determine its method considering professional ethics, codes and standards.	PO8	√	
CO5	Adopt modern engineering resources and tools for the solution of the problem.	PO5	√	
CO6	Prepare management plan and budgetary implications for the solution of the problem.	PO11	√	
CO7	Analyze the impact of the proposed solution on health, safety, culture and society.	PO6	√	
CO8	Analyze the impact of the proposed solution on environment and sustainability.	PO7	√	
CO9	Develop a viable solution considering health, safety, cultural, societal and environmental aspects.	PO3		√
CO10	Work effectively as an individual and as a team member for the accomplishment of the solution.	PO9	√	√
CO11	Prepare various technical reports, design documentation, and deliver effective presentations for demonstration of the solution.	PO10	√	√

CO12	Recognize the need for continuing education and participation in professional societies and meetings.	PO12		√

CO–PO Mapping and Explanation

The mapping between Course Outcomes (COs) and Program Outcomes (POs) for the thesis titled 'Design and Performance Analysis of FinFET Based Digital Circuits.' Each CO–PO relationship is explained in terms of how it supports the objectives and outcomes of the thesis.

CO–PO	Mapped Outcome	Explanation of Alignment with Thesis Objectives
CO1 – PO1	Apply EEE knowledge to solve complex engineering problems	Applied semiconductor and circuit theory to design and analyze FinFET structures, addressing short-channel effects and threshold voltage control.
CO2 – PO2	Identify contemporary real-life EEE problems	Reviewed recent FinFET research to identify challenges like leakage, delay, and scalability in nanoscale device design.
CO3 – PO4	Determine functional requirements through analysis and synthesis	Defined performance parameters such as PDP, leakage current, and delay, validating them through simulation results.
CO4 – PO8	Select solutions considering ethics, codes, and standards	Ensured all research followed professional and academic integrity, using validated models and proper citations.
CO5 – PO5	Adopt modern engineering tools and techniques	Utilized Silvaco TCAD, Cadence Virtuoso, and HSPICE for device and circuit simulations, showcasing proficiency in modern tools.
CO6 – PO11	Prepare management plan and budgetary implications	Planned simulations, optimized parameters, and managed computational resources effectively throughout the project.

CO7 – PO6	Analyze impact on health, safety, culture, and society	Developed energy-efficient circuits that reduce heat and power usage, contributing to safer electronic systems.
CO8 – PO7	Analyze environmental and sustainability impact	Demonstrated reduction of energy consumption and power leakage, promoting sustainable semiconductor technology.
CO9 – PO3	Develop viable solutions with societal and environmental awareness	Proposed FinFET-based low-power circuit solutions balancing performance, efficiency, and sustainability.
CO10 – PO9	Work effectively as individual and team member	Collaborated as a three-member team, coordinating tasks in simulation, analysis, and documentation.
CO11 – PO10	Prepare technical reports and presentations	Created detailed technical documentation, simulation graphs, and comparative analysis results for academic presentation.
CO12 – PO12	Recognize need for continuing education and participation	Explored emerging FinFET, CNFET, and leakage reduction techniques, promoting lifelong learning and professional growth.

Program Outcomes (POs) Mapping

The following table presents the **Program Outcomes (POs)** that can be addressed through the Project and Thesis work. The relevant POs are indicated by a tick (✓) mark in the table.

	Statement	Different Aspects	Put Tick (√)
PO3	Design/development of solutions: Design solutions for complex electrical and electronic engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.	Public health	
		Safety	
		Cultural	
		Societal	
		Environmental	√
PO4	Investigation: Conduct investigations of complex electrical and electronic engineering problems using research-based knowledge and research methods including design of experiments, analysis and	Design of experiments	√
		Analysis and interpretation of data	√

	interpretation of data, and synthesis of information to provide valid conclusions.	Synthesis of information	√
PO6	The engineer and society: Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to professional engineering practice and solutions to complex electrical and electronic engineering problems.	Societal	
		Health	
		Safety	
		Legal	
		Cultural	
PO7	Environment and sustainability: Understand and evaluate the sustainability and impact of professional engineering work in the solution of complex electrical and electronic engineering problems in societal and environmental contexts.	Societal	
		Environmental	
PO8	Ethics: Apply ethical principles embedded with religious values, professional ethics and responsibilities, and norms of electrical and electronic engineering practice.	Religious values	
		Professional ethics and responsibilities	√
		Norms	
PO10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	Comprehend and write effective reports	√
		Design documentation	
		Make effective presentations	
		Give and receive clear instructions	√
PO11	Project management and finance: Demonstrate knowledge and understanding of engineering management principles and economic decision making and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	Engineering management principles	
		Economic decision making	
		Manage projects	√
		Multidisciplinary environments	

Knowledge Profile (K3–K8) Mapping

The following table presents the **Knowledge Profile attributes (K3–K8)** that can be addressed through the Project and Thesis work. The relevant attributes are indicated by a tick (✓) mark in the table.

K	Knowledge Profile (Attribute)	Put Tick (√)
K3	A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline	√
K4	Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline	√
K5	Knowledge that supports engineering design in a practice area	√
K6	Knowledge of engineering practice (technology) in the practice areas in the engineering discipline	√
K7	Comprehension of the role of engineering in society and identified issues in engineering practice in the discipline: ethics and the engineer's professional responsibility to public safety; the impacts of engineering activity; economic, social, cultural, environmental and sustainability	
K8	Engagement with selected knowledge in the research literature of the discipline	√

Explanation or Justification of Knowledge Profiles (K3–K8)

The following section provides an **explanation or justification** of how the **Knowledge Profile attributes (K3–K8)** are addressed in **EEE 4700** and **EEE 4800** (Project and Thesis). Each attribute is explained in terms of its relevance and how it is achieved through the various stages of the project and thesis work.

K	Explanation/Justification
K3	This project builds upon fundamental concepts in semiconductor physics and circuit design, using theory-based frameworks such as MOSFET device modeling, short-channel effects, and logic design principles
K4	Exploration of advanced theoretical frameworks, such as electrostatic control in multi-gate devices and new logic styles optimized for FinFETs.
K5	By exploring various logic styles and analyzing their performance through SPICE simulations, the research supports practical engineering design aimed at enhancing efficiency and reliability.
K6	The use of simulation tools such as TCAD and SPICE represents the practical application of engineering technology

K8	The project is rooted in a thorough review of current research on FinFET device physics, advanced logic styles, and circuit optimization techniques

Ranges of Complex Engineering Problem Solving (P1–P7) Mapping

The following table presents the **Attributes of the Ranges of Complex Engineering Problem Solving (P1–P7)** that can be addressed through the Project and Thesis work.

The relevant attributes are indicated by a tick (✓) mark in the table.

P	Range of Complex Engineering Problem Solving	Put Tick (√)
Attribute	Complex Engineering Problems have characteristic P1 and some or all of P2 to P7:	
Depth of knowledge required	**P1:** Cannot be resolved without in-depth engineering knowledge at the level of one or more of K3, K4, K5, K6 or K8 which allows a fundamentals-based, first principles analytical approach	√
Range of conflicting requirements	**P2:** Involve wide-ranging or conflicting technical, engineering and other issues	√
Depth of analysis required	**P3:** Have no obvious solution and require abstract thinking, originality in analysis to formulate suitable models	√
Familiarity of issues	**P4:** Involve infrequently encountered issues	
Extent of applicable codes	**P5:** Are outside problems encompassed by standards and codes of practice for professional engineering	
Extent of stakeholder involvement and conflicting requirements	**P6:** Involve diverse groups of stakeholders with widely varying needs	√
Interdependence	**P7:** Are high level problems including many component parts or sub-problems	

Explanation or Justification of Ranges of Complex Engineering Problem Solving (P1–P7). The following section provides an **explanation or justification** of how the **attributes of the Ranges of Complex Engineering Problem Solving (P1–P7)** are addressed in **EEE 4700** and **EEE 4800** (Project and Thesis).

Each attribute is explained in terms of its application and relevance throughout the project and thesis activities.

P	Explanation/Justification
P1	The analysis relies on a first-principles approach to modeling FinFET behavior using TCAD and SPICE simulations, integrating theoretical frameworks with practice-oriented solutions. The study is grounded in and contributes to the current state of knowledge in the discipline.
P2	The thesis tackles the trade-offs between performance metrics such as power, delay, and area efficiency, which often conflict in digital circuit design.
P3	Abstract thinking is essential to understand the interactions between device- and circuit-level phenomena and to develop performance optimization strategies.
P6	Some fields require the FinFET devices to be as fast as possible, while some fields require that the power consumption is as low as possible. Therefore, there's always some trade-offs and the needs are widely varying.

Ranges of Complex Engineering Activities (A1–A5) Mapping

The following table presents the **Attributes of the Ranges of Complex Engineering Activities (A1–A5)** that can be addressed through the Project and Thesis work.

The relevant attributes are indicated by a tick (✓) mark in the table.

A	Range of Complex Engineering Activities	Put Tick (√)
Attribute	Complex activities means (engineering) activities or projects that have some or all of the following characteristics:	
Range of resources	**A1:** Involve the use of diverse resources (and for this purpose resources include people, money, equipment, materials, information and technologies)	√
Level of interaction	**A2:** Require resolution of significant problems arising from interactions between wide-ranging or conflicting technical, engineering or other issues	√
Innovation	**A3:** Involve creative use of engineering principles and research-based knowledge in novel ways	√
Consequences for society and the environment	**A4:** Have significant consequences in a range of contexts, characterized by difficulty of prediction and mitigation	
Familiarity	**A5:** Can extend beyond previous experiences by applying principles-based approaches	

Explanation or Justification of Ranges of Complex Engineering Activities (A1–A5)

The following section provides an **explanation or justification** of how the **attributes of the Ranges of Complex Engineering Activities (A1–A5)** have been addressed in **EEE 4700** and **EEE 4800** (Project and Thesis).

Each attribute is explained based on its relevance and how it has been demonstrated through the project and thesis work.

A	Explanation/Justification
A1	Requires people, software tool, information about the device and technologies to implement features of the Device and simulate the performance.
A2	Conflicting issues such as the issue of speed, power dissipation, scaling has to be resolved.
A3	To solve many issues that has been addressed, thinking outside the box becomes necessary. This also requires creative use of novel technologies.

Chapter 9

Conclusion

The continuous miniaturization of transistor dimensions has created significant challenges for traditional planar MOSFETs, primarily due to short-channel effects, excessive leakage currents, and degraded electrostatic control. Our thesis focused on the design and performance analysis of digital logic circuits implemented using FinFET and CNFET technologies, comparing their behavior against conventional CMOS circuits. Through comprehensive simulation and evaluation, it was demonstrated that FinFET technology, with its three dimensional multi-gate architecture, effectively overcomes the limitations of planar CMOS by offering superior leakage reduction, scalability, and switching efficiency **[2]**. These attributes establish FinFET as the current benchmark for nanoscale integrated circuit design and a robust platform for the semiconductor industry's ongoing device scaling.

Detailed device and circuit-level analyses revealed the fact that the transition from CMOS to FinFET leads to substantial performance increase in terms of static power, propagation delay, and power delay product (PDP). In our simulations in Cadence Virtuoso, FinFET circuits achieved leakage power reductions which exceeded 90% and displayed faster switching characteristics due to enhanced gate control and minimized short-channel effects **[2]**.

The CNFET technology, employing carbon nanotubes as the channel material, demonstrated even greater theoretical efficiency, achieving extremely low leakage currents **[7]**. However, despite these advantages, CNFET which is still in experimental stage, faces manufacturing challenges and material reliability issues, which currently limit its large-scale practical adaptation. Hence, while CNFET holds promise for future nanoelectronics, FinFET remains the most viable and industry-ready solution at present context.

To further mitigate leakage power, two established circuit-level leakage control techniques: LECTOR and INDEP were implemented and analyzed across CMOS, FinFET, and CNFET devices. The LECTOR technique, which introduces cross-coupled leakage control transistors between the pull-up and pull-down networks, consistently provided stable leakage reduction with minimal delay penalty, making it both practical and efficient. On the other hand, the INDEP technique, which regulates leakage through input-dependent gate biasing, achieved aggressive static power reduction (often on the order of 90% or more) **[5]**, but this came at the cost of increased delay and degraded PDP in several circuit configurations. The comparative findings clearly indicate that LECTOR offers a superior tradeoff between leakage control and performance retention for most high-speed designs, whereas INDEP, though powerful in reducing leakage, is more suitable for low-power designs where timing constraints are not that significant.

Across technologies, FinFET circuits integrated with LECTOR demonstrated the most consistent and desirable performance profile, achieving significant leakage reduction without sacrificing switching speed or energy efficiency. This excellent synergy between FinFET's structural efficiency and LECTOR's self-regulated leakage control mechanism makes the combination an ideal candidate for next-generation low-power VLSI designs. While CNFET-based circuits, particularly those utilizing LECTOR, exhibited excellent potential for ultra-low-power operation, their various challenges remain barriers to immediate adaptation. Conversely, CMOS circuits whether optimized or not continue to lag behind due to inherent structural and scaling constraints.

In conclusion, our research validates FinFET technology as the most efficient and practical advancement beyond planar CMOS,becoming an optimal balance between power efficiency, speed, and manufacturability **[2]**. Among the leakage mitigation methods studied, LECTOR emerges as the most reliable and design-friendly approach, providing consistent power savings with limited trade-offs in delay and performance. INDEP remains a valuable alternative for applications with strict power constraints and relaxed timing requirements. The combined study of FinFET architectures and leakage mitigation techniques emphasizes the vital role of device innovation and circuit-level optimization in achieving the dual objectives of high performance and energy efficiency in nanoscale VLSI systems.

For future research, our work can be extended to explore more complex digital architectures, such as arithmetic units, memory arrays, and sequential logic. Integrating machine learning-based design optimization could enhance parameter tuning and circuit adaptability. Furthermore, hybrid configurations combining FinFET and emerging materials (such as CNFET, GNRFET, or TFET) may pave the way for the next generation of ultra-low-power, high-performance semiconductor technologies operating below the 5 nm scale.

References

[1] T. Shan, “Advantages of FinFET over traditional CMOS: Reasons and implications,” Theoretical and Natural Science, vol. 14, pp. 219-223, 2023. https://doi.org/10.54254/2753-8818/14/20241010

[2] Maurya, R.K., Bhowmick, B. Review of FinFET Devices and Perspective on Circuit Design Challenges. Silicon 14, 5783–5791 (2022). https://doi.org/10.1007/s12633-021-01366-z

[3] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," in Proceedings of the IEEE, vol. 91, no. 2, pp. 305-327, Feb. 2003.https://doi.org/10.1109/JPROC.2002.808156

[4] N. Hanchate and N. Ranganathan, “LECTOR: a technique for leakage reduction in CMOS circuits,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 2, pp. 196-205, 2004. https://doi.org/10.1109/TVLSI.2003.821547

[5] V. K. Sharma, M. Pattanaik, and B. Raj, “INDEP approach for leakage reduction in nanoscale CMOS circuits,” Int. J. Electronics, vol. 102, no. 2, pp. 200-215, 2015. https://doi.org/10.1080/00207217.2014.896042

[6] Mushtaq, U., Sharma, V.K. Performance analysis for reliable nanoscaled FinFET logic circuits. Analog Integr Circ Sig Process 107, 671–682 (2021). https://doi.org/10.1007/s10470-020-01765-z

[7] M. H. Fuad, M. F. Nayan, S. S. Noor, R. Yeassin, and R. R. Mahmud, “Comprehensive performance analysis of CMOS and CNTFET based 8T SRAM cell,” Journal of Electronic Science and Technology, vol. 23, no. 2, Art. no. 100306, 2025. https://doi.org/10.1016/j.jnlest.2025.100306

[8] S. V. Yamani, H. K. R. V. Kudulla and S. S. Rao, "Design of Three Stage Dynamic Comparator with Tail Transistor using 20nm FinFET Technology for ADCs," 2022 International Conference on Computing, Communication and Power Technology (IC3P), Visakhapatnam, India, 2022, pp. 32-37 https://doi.org/10.1109/IC3P52835.2022.00016

[9] Gupta, R. Mathur, and M. Nizamuddin, “Design, Simulation and Comparative Analysis of a Novel FinFET-Based Astable Multivibrator,” AEÜ – International Journal of Electronics and Communications, 2019 https://doi.org/10.1016/j.aeue.2018.12.007

[10] Verma, S., Tripathi, S.L. Design and Analysis of Heterojunction Inverted-T P-FinFET on 14nm Technology Node for Use in Low-Power Digital Circuits. Silicon 15, 3725–3736 (2023). https://doi.org/10.1007/s12633-023-02294-w

[11] M. Susaritha and J. Senthilkumar, “Design and Analysis of High Performance FinFET-Based Linear Feedback Shift Register for Cryptography Applications,” *Journal of Nanoelectronics and Optoelectronics*, vol. 19, no. 6, pp. 588–599, Jun. 2024, doi: 10.1166/jno.2024.3613

[12] S. S. Zaman, P. Kumar, M. P. Sarma, A. Ray and G. Trivedi, "Design and Simulation of SF-FinFET and SD-FinFET and Their Performance in Analog, RF and Digital Applications," 2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), Bhopal, India, 2017, pp. 200-205, doi: https://doi.org/10.1109/iNIS.2017.49

[13] A. Lazzaz, K. Bousbahi, and M. Ghamnia, “Performance Analysis of FinFET-Based Inverter, NAND and NOR Circuits at 10 nm, 7 nm and 5 nm Node Technologies,” Facta Universitatis – Series: Electronics and Energetics, vol. 36, no. 1, pp. 1–16, 2023. https://doi.org/10.2298/FUEE2301001L

[14] G. Vasudeva, M. Jatkar, T. R. Kulkarni, R. R. Kulkarni, B. Gururaj, and T. M. P., “Design of FinFET Based Op-Amp Using High-K Device 22 nm Technology,” Advances in Transdisciplinary Engineering, pp. 928–939, 2023. https://doi.org/10.3233/ATDE231033

[15] Ul Haq, S., Sharma, V.K. Energy-Efficient Design for Logic Circuits Using a Leakage Control Configuration in FinFET Technology. J. Inst. Eng. India Ser. B 105, 903–911 (2024). https://doi.org/10.1007/s40031-024-01026-x

[16] Kajal and V. K. Sharma, “Study of the Reliability for the Leakage Mitigation Methods Using FinFETs,” Recent Advances in Electrical & Electronic Engineering, vol. 16, no. 7, pp. 697–708, Apr. 2023. https://doi.org/10.2174/2352096516666230414134447

[17] N. E. I. Boukortt, T. R. Lenka, S. Patanè, and G. Crupi, “Effects of Varying the Fin Width, Fin Height, Gate Dielectric Material, and Gate Length on the DC and RF Performance of a 14-nm SOI FinFET Structure,” Electronics, vol. 11, no. 1, p. 91, 2022. https://doi.org/10.3390/electronics11010091

[18] V. K. Sharma, M. Pattanaik, and B. Raj, “PVT variations aware low leakage INDEP approach for nanoscale CMOS circuits,” Microelectronics Reliability, vol. 54, no. 1, pp. 90-99, 2014, doi: https://doi.org/10.1016/j.microrel.2013.09.018

[19] R. R. Vallabhuni, G. Yamini, T. Vinitha and S. S. Reddy, "Performance analysis: D-Latch modules designed using 18nm FinFET Technology," 2020 International Conference on Smart Electronics and Communication (ICOSEC), Trichy, India, 2020, pp. 1169-1174, doi: https://doi.org/10.1109/ICOSEC49089.2020.9215341