ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)

ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION SUMMER SEMESTER, 2023-2024

DURATION: 2 HOURS FULL MARKS: 120

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

Answer **all 4 (four)** questions. Figures in the right margin indicate full marks of questions with corresponding COs and POs in parentheses.

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1. a) Design a 5-to-32 decoder using 3-to-8 decoders. You may use additional combinational circuits (such as logic gates) if needed to make the circuit functional. Make sure to include the following in your diagram: — 10 (CO1) (PO1)

   - Clearly show the 5 input lines.
   - Represent all 32 outputs (you can group them, e.g., O_0 to O_7, O_8 to O_{15}, etc.).
   - Use block diagrams to represent each 3-to-8 decoder.
   - Indicate which input combinations activate each decoder and the corresponding output range it produces (Showing the whole Truth Table is not required).

   b) A 3-bit binary comparator compares two binary numbers $A = A_2A_1A_0$ and $B = B_2B_1B_0$, and produces three outputs: — 3 + 9 (CO1) (PO1)

   $$A > B, \quad A < B, \quad A = B$$

   i Write the Boolean expressions for all three outputs (a circuit diagram is not necessary).

   ii Briefly justify the correctness of these expressions by verifying them for any three input combinations one for each case: $A > B$, $A < B$, and $A = B$. For each case, show all three outputs.

   c) You are provided with a Programmable Logic Device (PLD) where the AND array is programmable, but the OR array is fixed. In the PLD structure shown in Figure 1, the symbol (+) indicates that the wires are **not connected**, the symbol (×) indicates a **programmable connection** (which you are allowed to make), and the symbol (•) represents a **fixed junction connection**. — 1 + 7 (CO3) (PO2)

   Your task is to make the necessary programmable connections (using ×) in the AND array section of the PLD to implement the following two functions:

   $$F_1 = \sum m(0, 1, 2, 4, 5, 8, 14, 15)$$

   $$F_2 = \sum m(0, 1, 8, 9, 14, 15)$$

   What kind of PLD is shown in Figure 1 (PAL, PLA, or ROM)? Identify the type and make the necessary programmable connections to complete the circuit. You are allowed to simplify the functions if required before implementation.

2. a) Race Around Condition is a phenomenon observed in certain types of flip-flops under specific conditions.

   i. Define the Race Around Condition. — 2 (CO1) (PO1)

   ii. How does the Race Around Condition differ from normal toggling? — 2 (CO1) (PO1)

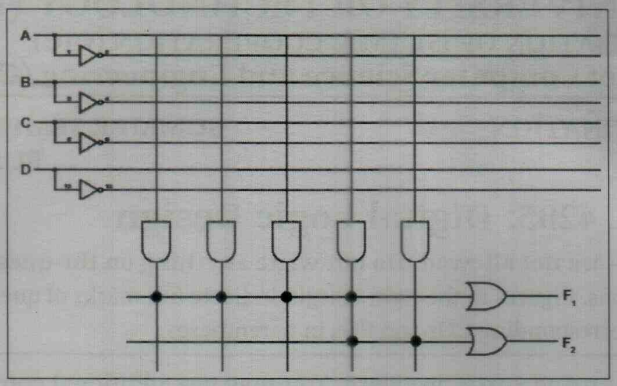

Figure 1: A PLD

iii. Which type of flip-flop suffers from this problem? 1 (CO1) (PO1)

iv. Draw the circuit diagram of the flip-flop and explain the specific case in which the Race Around Condition occurs. You may describe the behavior using different possible cases based on previous and intermediate outputs and their effect on the next state, or a timing diagram. Your explanation must be clear and supported by proper logic. 6 (CO1) (PO1)

v. How does introducing propagation delay help mitigate the Race Around Condition? Will increasing the delay always resolve the issue? Justify your answer. 3 (CO1) (PO1)

b) You are given a memory element (Flip-Flop A) that has a single input and a clock signal. On the rising edge of the clock, the output of this element simply takes the value of its input.

You have to design a circuit using Flip-Flop A and any necessary logic gates to replicate the behavior of another type of flip-flop (Flip-Flop B), which has two inputs:

- When the first input is high and the second is low, the output becomes high.
- When the first input is low and the second is high, the output becomes low.
- When both inputs are low, the output retains its previous state.
- The case when both inputs are high is considered invalid.

Answer the following questions based on the provided scenario:

i. Identify Flip-Flop A and Flip-Flop B based on their described behaviors. 2 (CO1) (PO1)

ii. Write the required characteristic table and the excitation table and clearly mention which flip flop they belong to. 5 + 3 (CO1) (PO1)

iii. Using the information from Question 2.b)ii, create a merged table and derive the characteristic equation(s) required to implement the required flip flop. 4 (CO1) (PO1)

iv. Draw the block diagram of the resulting circuit, clearly showing the original flip-flop and any additional logic you have used. 2 (CO5) (PO3)

3. a) Why are D flip flops usually used in registers but T flip flops are used for counters? 4 (CO1) (PO1)

b) Bi-directional shift registers are registers that can shift data in both directions: left to right and right to left. Now answer the following questions:

i. Design a 4-bit bidirectional shift register and briefly describe its key components. 7 (CO1) (PO1)

ii. Take any two random 4-bit binary numbers and demonstrate how the bidirectional shift register operates in both left and right shift modes. Clearly show: 6 (CO3) (PO2)

- The state of the register at each clock cycle,
- The direction of shifting for each case, and
- The mode and input used.

You may use a table, timing diagram, or any other clear and understandable representation.

c) Universal Shift Registers are sequential logic circuits capable of performing multiple operations such as shift left, shift right, parallel load, and hold (no change), based on control inputs. Design a 4-bit Universal Shift Register that performs the following operations based on the mode control inputs as shown in Table 1. 8 + 5 (CO1) (PO1)

Table 1: Mode control and corresponding register operations

Mode Control		Register Operation
S1	S0	
0	0	Shift Left
0	1	Shift Right
1	0	Parallel Load
1	1	No Change

Your answer must include -

- A **clear, labeled diagram** of the circuit, with **required number of flip-flops and multiplexers** and all component **labels** (MUX and flip-flop inputs, clock inputs, and outputs).
- A **short justification** (1–2 lines) for each mode of operation explaining how the circuit behaves for each combination.

4. a) Draw the circuit diagram of an asynchronous BCD up counter. Briefly explain the changes necessary to convert a 16-bit asynchronous up counter into a BCD counter, and justify why these changes are needed. 5 + 2 (CO5) (PO3)

b) Design a synchronous sequential circuit that generates the following sequence: 1+2+ 6+4+ 7+3 (CO5) (PO3)

$$1 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 0 \rightarrow 2 \rightarrow 4 \rightarrow 6$$

This includes all odd numbers from 0 to 7, followed by all even numbers.

Your answer must include:

i. The type of flip-flop used and the count of number of flip-flops required.

ii. The excitation table of the selected flip-flop.

iii. A combined state table showing Present state, Next State and Inputs required for each flip-flop.

iv. The derived input equations for each flip-flop.

v. The circuit diagram.

vi. A brief logical justification for the obtained input equations.