
بسماللهالرحمنالرحيم

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# DESIGN AND IMPLEMENTATION OF DIGITAL CONTROLLERS FOR BUCK CONVERTER USING LINEAR AND NONLINEARCONTROL METHODS

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# CERTIFICATE OF APPROVAL

Certified that the project dissertation entitled

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In the end we would like to show our deepest respect to our parents, family, friends and all those who showed patience and tenacity with us to finish with success.

*Dedicated to*

*My Dear Parents*

*Who supported me to fly when I was an Eaglet.*

# ABSTRACT

DC-DC power converters play an important role in powering telecom and computing systems. With the speed improvement and cost reduction of digital control, digital controller is becoming a trend for DC-DC converters in addition to existed digital monitoring and management technology. In this thesis, digital control is investigated for DC-DC converters applications.

To deeply understand the whole control systems, DC-DC converter models are investigated based on averaged state-space modeling. Considering Buck DC-DC converter, the thesis takes it as an example for digital control modeling and implementation.

In Chapter 3, unified steady-state DC models and small-signal models are developed for DC-DC buck converters. Based on the models, digital controller design is implemented. In Chapter 4, digital modeling platforms are established based on Matlab, Digital PID design and corresponding simulation results are provided. Also some critical issues and practical requirements are discussed. In Chapter 6, a DSP-based digital controller is implemented with the TI's DSP chip TMS320F2812. Related implementation methods and technologies are discussed.

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# 1. INTRODUCTION

## 1.1 Objective of the Research Work

Switched mode power supplies (SMPSs) are needed to convert electrical energy from one voltage level to another. SMPSs are widely used in DC-DC conversions, where the input is a DC voltage that can be, for example, a rectified line voltage, an output voltage of a power factor correction (PFC) circuit, a battery or fuel cell voltage.

In such power conversions, DC-DC converters operate at relatively high switching frequencies, and this enables the use of small inductive components which improve the dynamic behavior and reduce the size of the converter.

Despite the above-mentioned benefits of SMPSs, there are several parameters, which are not desired and have a strong influence on the converters behavior, being mainly:

- Non-linear components in the converter structure,
- Line and load variations, and
- Electro-magnetic interferences (EMI).

The DC-DC converter has non-linear components (capacitors, inductors, and resistors), the value of which changes non-linearly if the converter is disturbed or may change within time. The effects of these converter parameters variations are given in [6].

For the design of a DC-DC converter, a nominal input voltage and load values are suggested. In practice, these nominal values may deviate. For example, 20% line variation is expected or the nominal load may deviate to no-load or full load. These phenomena are studied in [1-6].

The purpose of electro-magnetic interference (EMC) is to ensure that an electronic system can operate in its electromagnetic environment without responding to electrical noise or generating unwanted electrical interference. For example, in DC-DC power supply EMI has an influence on the converter component. The EMI effects on the DC-DC converter are studied in [7].

These parameters force the converter to deviate from the desired operating condition. If

the parameter deviation increases, this will cause the converter not to operate in steady state. Many control methods are used to control SMPSs and solve the problem mentioned above. Each control method has its own advantages and drawbacks due to which that particular control method appears to be the most suitable control method under specific conditions, compared to other control methods. It is always demanded to obtain a control method that has the best performances under any conditions.

The thesis defines the causes by which the selecting of a specific control method is influenced, i.e. the fuzzy PID control (FPID), over other control methods. A detailed research analysis is done for the FPID controller.

The research work is done in following logical sequence:

- Study of the DC-DC converter topologies,
- Study of the control methods used to control the DC-DC converters,
- Study of the traditional PID control as one control method,
- Study of the Fuzzy logic control as a second control method,
- Proposed a self-tuning FPID controller for the control of Buck Converter.

It is noticed that the influence of the FPID on the behavior of the converter in steady state and under dynamic conditions is better than that of the PID control and fuzzy logic control.

The FPID is applied to the DC-DC buck converter and the response of the converter is analyzed in steady state and under dynamic conditions.

The research work process can be described as follows:

In chapter two, linear power supply is analyzed and its advantages and drawbacks are discussed. In the next section, SMPSs are studied in detail and their benefits and drawbacks over linear regulators are shown. A classification of SMPSs into isolated and non-isolated DC/DC converters is given. In last section of the chapter the feedback control system is summarized.

Chapter three focuses on analyzing the topology and operation of the DC-DC buck converter. The modeling of the topology, including steady state average model and small-signal dynamic model, are established and the related controller compensation design issues are addressed based on the models and analysis.

Chapter four discusses digital and analog control, which includes the theory, methodology and critical issues of a digital and analog controller. As a case study, a digital and analog PID compensator is designed based on the specifications of the given power stage. Also, this chapter explores the modeling and simulation of a digital controller with DSPs.

In Chapter five fuzzy logic control is introduced based on that knowledge an intelligent self- tuning fuzzy PID controller is proposed for the control of buck converter. The fuzzy logic control is used to tune the proportional, integral and derivative gain of the conventional PID controller based on certain function of the error signal to obtain stable and fast transient response in-spite of changes in load and source sides.

Chapter six explores DSP implementation of a digital controller, which brings in the introduction of DSP chips, to be specific, TI C24X and TMS320F2812. Then, the PWM generators and ADC of TMS320F2812 are emphasized as the important devices in the controller. Controller implementation based on the TMS320F2812 is described as one of the important part of the thesis.

Chapter seven provides and analyzes the experimental results of closed-loop and open loop system. It should be noted that the overall performance of the closed system is improved significantly

In chapter eight, the conclusions obtained from the research work are given. The main contribution of this thesis is summarized and suggestions for future research work are given.

# CHAPTER 2
# DC-DC POWER SUPPLIES

# 2. DC-DC POWER SUPPLIES

## 2.1 Introduction

With the introduction of the transistor in the early 1950's and, especially, with the development of integrated circuits from the early 1960's onwards (Josephson 1967), designers of electronic equipment, computers and instrumentation increasingly have brought up the demand for smaller, more efficient power sources to supply their equipment. Therefore, to meet these demands, the power supply itself has become more and more sophisticated. In fact, the development in power supply technology can be directly linked to the introduction of various power semiconductor devices, even though the theory, in many cases, was already well known.

The regulated power supply technology can be divided into two distinct forms: firstly, the linear regulator which can be either a series or parallel regulator and, secondly, the switched-mode conversion technique. Switched-mode technology is multi-facetted with a wide variety of topologies achieving the result of providing a regulated DC voltage.

The main difference between the linear and switched-mode regulator is in efficiency. The linear regulator utilizes simple techniques of controlled energy dissipation to achieve a regulated output voltage independent of line and load variations. It is, therefore, inherently inefficient, especially when a wide input voltage range has to be applied. When linear techniques are applied to regulate a low voltage from the mains (110V or 240V AC source) then the disadvantages of the technique become apparent.

## 2.2 Linear Power Supply

Linear power supplies provide significant advantages over switching regulators in:

- Simplicity,
- Cost, and
- Output noise.

A typical linear power supply is shown in Figure 2.1, which has the following disadvantages

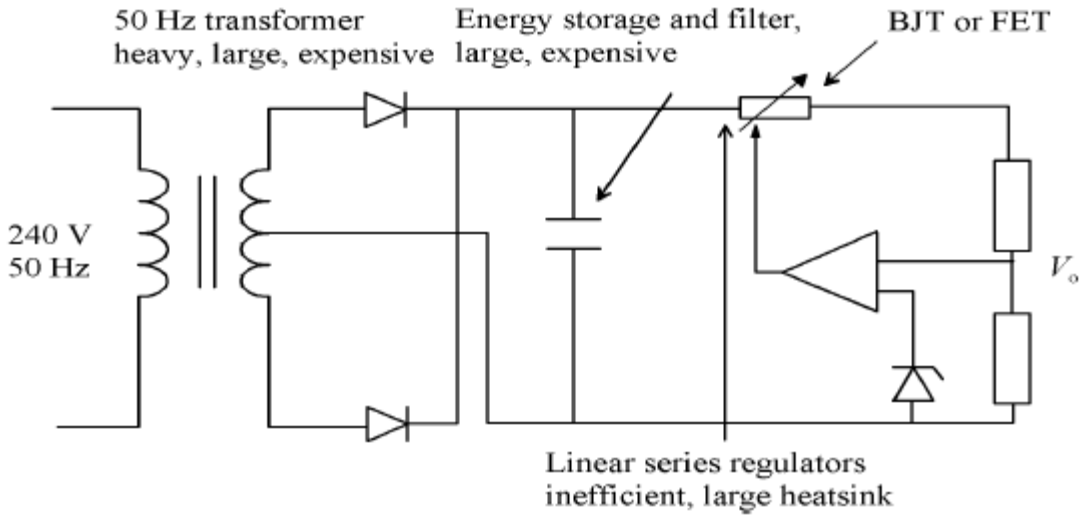


**Figure 2.1: Practical linear series regulator circuit.**

- The main transformer operating at a low frequency is heavy, large and expensive,
- Large heat-sinking is required to dissipate the heat generated by the regulating element, and
- The efficiency is low.

Two major types of linear regulators are considered and shown in Figure 2.2. The simple series regulator in Figure 2.2.a is a transistor connected as an emitter follower (or source follower in FET). The transistor operates in its linear active region rather than a switch. The emitter voltage $V_o$ becomes a function of $V_{control}$ rather than the input voltage or the load current and the term linear regulator is appropriate to describe the circuit. The power loss and efficiency are:

$$P_{loss} = (V_{in} - V_o)I_{load}, \quad (2.1)$$

$$\eta = \frac{V_o I_{load}}{V_{in} I_{load}} = \frac{V_o}{V_{in}}. \quad (2.2)$$

The shunt regulator shown in Figure 2.2.b resembles a common emitter amplifier circuit. The transistor, once again, is used in the linear active region. The collector current will be $\beta I_b$ rather than the function of the load current. Again, the output is a linear function of the control,

and the circuit is another example of a linear regulator. The losses and efficiency for the shunt regulator are:

$$P_{\text{loss}} = V_{\text{o}} I_{\text{c}} + \left(I_{\text{load}} + I_{\text{c}}\right)^2 R_{\text{c}}, \tag{2.3}$$

$$\eta = \frac{V_{\text{o}} I_{\text{load}}}{V_{\text{in}} \left(I_{\text{load}} + I_{\text{c}}\right)}. \tag{2.4}$$

With no load there is a significant loss because $I_c \neq 0$, and, in best the case where $I_{load} >> I_c$, the efficiency becomes $V_o/V_{in}$.

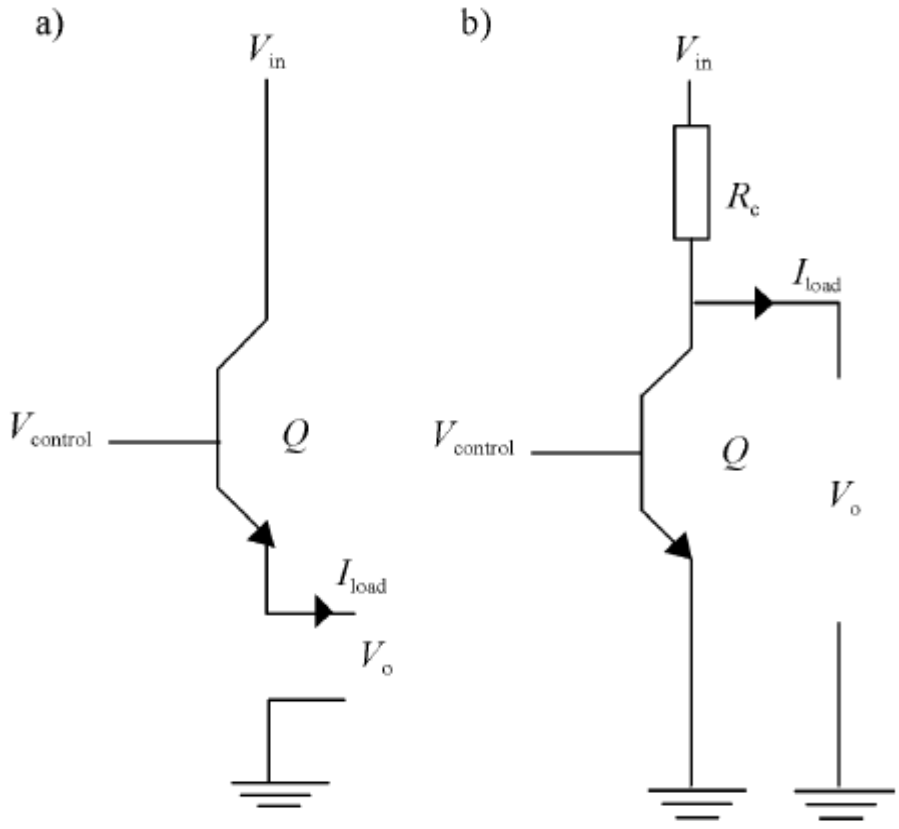


**Figure 2.2: Basic circuits for linear regulators. a) Series regulator, b) shunt regulator.**

Linear regulators acting as converters limit the efficiency. However, since they bring the possibility of perfect regulation, linear regulators are often used as elements of larger conversion systems.

## 2.3 Switched Mode Power Supply

Switched-mode power supply shown in Figure 2.3 offers the possibility of theoretically loss-less power conversion, which is not true in reality. The switched-mode regulator employs duty cycle control of a switching element to block the flow of energy and thus achieve regulation.

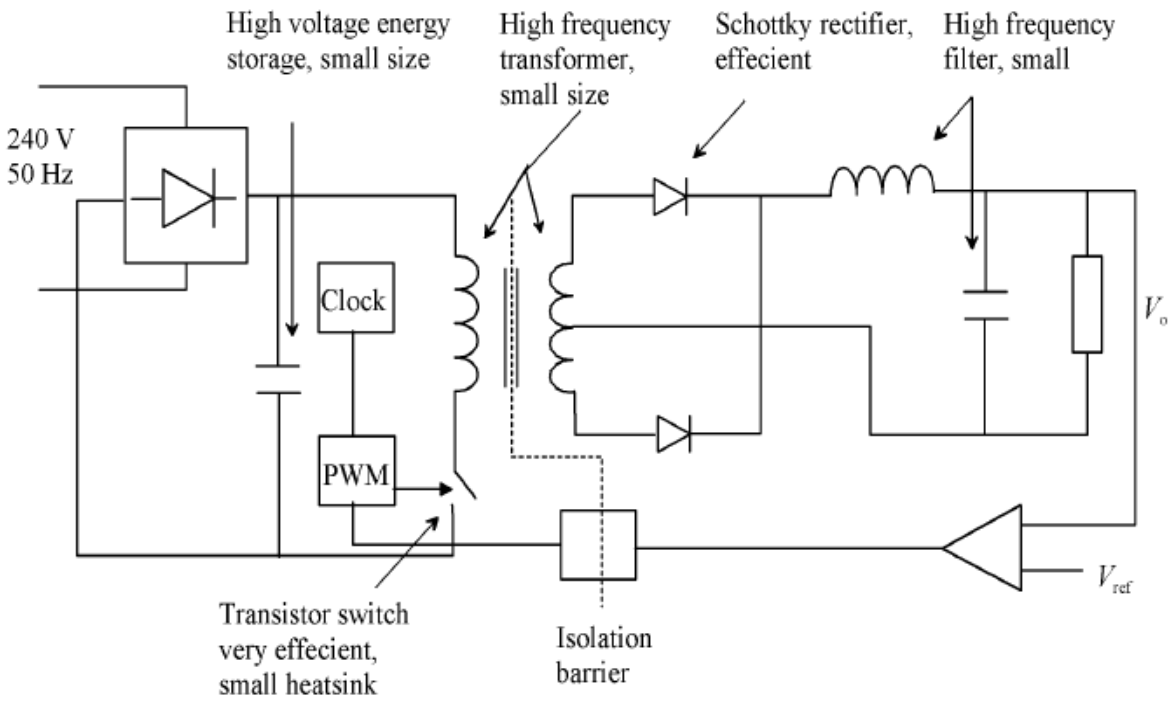


**Figure 2.3: Practical circuit of switch mode regulator**

The switched mode power supply has the following advantages compared to the linear regulator:

- High switching frequency enables the use of a small ferrite transformer core,
- since the rectified mains voltage is chopped, the energy storage for hold-up can be accomplished on the primary side of the step-down transformer, and smaller but high voltage capacitors than in the linear counterpart can be used,
- It can step the voltage up/down and reverse its polarity,
- It may operate in a much larger DC input voltage range than the linear regulators, and
- It often has a higher efficiency.

Although the benefits of switched-mode techniques are significant, there are some drawbacks:

- Both the input and output present increased noise of the supply due to the power switching techniques, and
- The associated control circuitry is more complicated compared to the linear counterpart, e.g. an isolated feedback signal is needed for the control.

Historically, the linear regulators were very common during the late 1950's and early 1960's when power supplies using switching techniques were very rare. The prevailing use of switched-mode power supplies is linked to the development of fast, high-voltage switching power transistors and, to a smaller extent, to the developments of ceramic ferrite materials and capacitor technology. Nowadays, switched mode power supplies are widely used.

However, linear regulators are still in use in applications for the following reasons:

- Linear regulators are simple,
- It is possible in some cases to reach a high efficiency with linear power supplies too. This is accurate if the current that powers the regulator is a small percentage of the current drawn from the output of the regulator. Thus, when the voltage of the source powering the linear regulator is near the output voltage of the regulator, the efficiency is high. In that case, the linear regulator may be a better alternative than the switching regulator, and
- They have been available for tens of years

## 2.4 Switched-Mode Power Supply Topologies

### 2.4.1 Non-isolated Topologies

With the upcoming commercial switched-mode power supply manufacturing industry during the 1970s, the theory and technology of switched-mode conversion was being re-nationalized as part of the academic discipline of power electronics.

The greatest contribution made within the discipline is by R.D. Middlebrook and his colleagues of the Power Electronics Group of Caltech in California, USA. The initial work of the Caltech Group, started in 1970 was performed with the aim of developing models for the three

DC-DC switching regulator topologies, the Buck, Boost and Buck-Boost converters (Haver1974), which were already developed in the 1960s.

From this work, the modeling and analysis method called state-space averaging was created (Pressman 1977). The state-space averaging allowed a theoretical prediction of the frequency response of a converter and, therefore, enabled a better understanding of the feedback loop and stability criteria of a switched-mode regulator.

Further work at Caltech, especially by Cuk in his PhD Thesis, produced a fourth topology of the basic DC-DC switching regulator, which the author described as an optimum topology (Cuk 1977) because of its symmetrical structure and non-pulsating input and output currents.

The new optimum topology DC-DC switching regulator is now commonly known as the Cuk converter, named after its inventor, and completes the family of single-switch non-isolated switching regulators.

The non-isolated DC/DC converters family shown in Figure 2.4 can be classified as follows:

- Buck converter (step down DC/DC converter),
- Boost converter (step up DC/DC converter),
- Buck-Boost converter (step up/down DC/DC converter, opposite polarity), and
- Cuk converter (step up/down DC/DC converter).

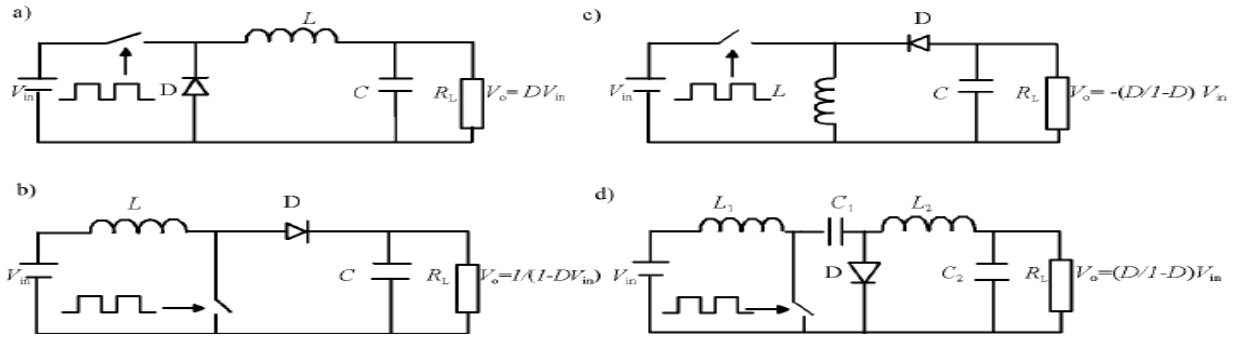


**Figure 2.4: Non- isolated DC/DC converter topologies a) Buck converter, b) Boost converter, c) Buck-Boost converter, and d) Cuk converter.**

### 2.4.2 Isolated Topologies

In many applications, isolation is a necessary requirement within the converter between input and output. By inserting isolation transformers into the four basic non-isolated switching regulator topologies, four single-ended isolated switching DC/DC converters can be obtained, shown in Figure 2.5:

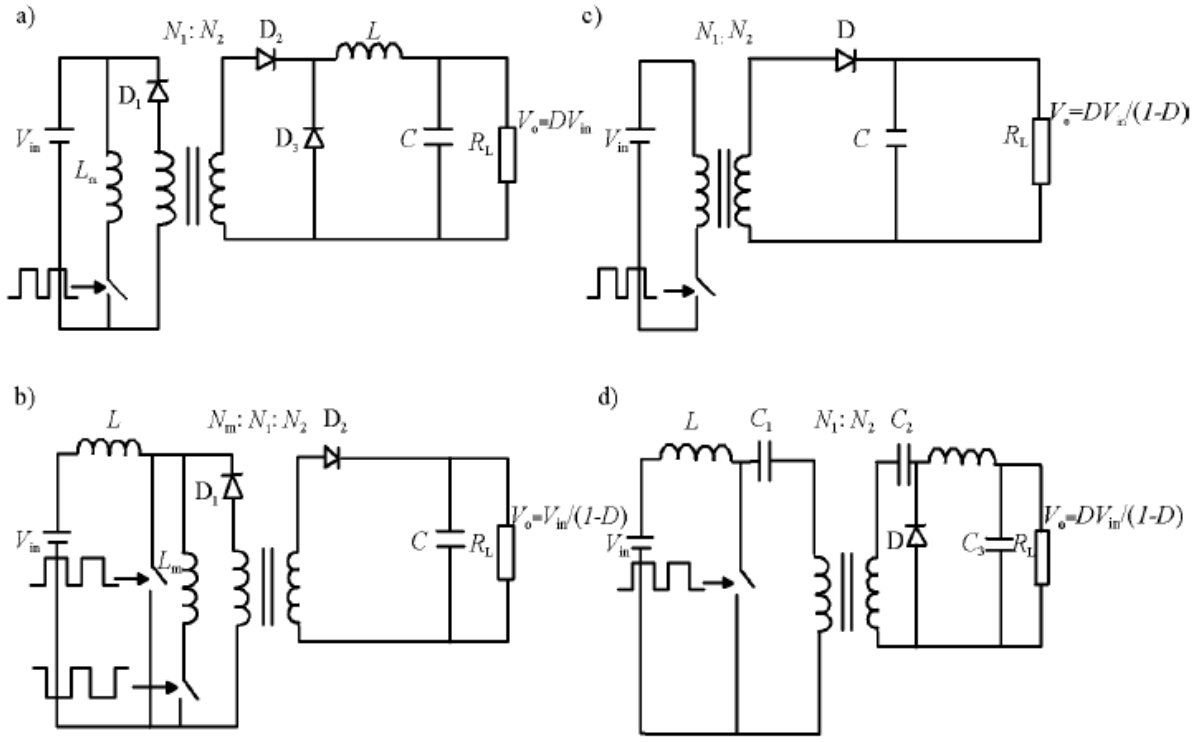


**Figure 2.5: Isolated DC/DC converter topologies a) Forward converter, b) Isolated Boost converter, c) Flyback converter, and d) Isolated Cuk converter.**

- The Forward converter (step down DC/DC converter),
- The Isolated Boost converter (step up DC/DC converter),
- The Flyback converter (step up/down DC/DC converter), and
- The Isolated Cuk converter (step up/down DC/DC converter).

The isolated DC/DC Buck and Buck-Boost topologies are more commonly referred to as the Forward and Flyback DC/DC converter respectively, and are the most used topologies in commercially manufactured switched-mode power supplies.

### 2.4.3 Multiple Switch Topologies

The main disadvantage of single switch topologies is that the transistor switch should be capable of high-voltage blocking (twice the DC input voltage), especially when operating from a rectified AC mains supply. The single switch topology is not an ideal solution for higher power converters either, since these converters need a higher current rating of the transistor switch. Therefore, another group of isolated DC/DC converters utilizing more than one switch can be identified. Figure 2.6 illustrates three multiple switch topologies:

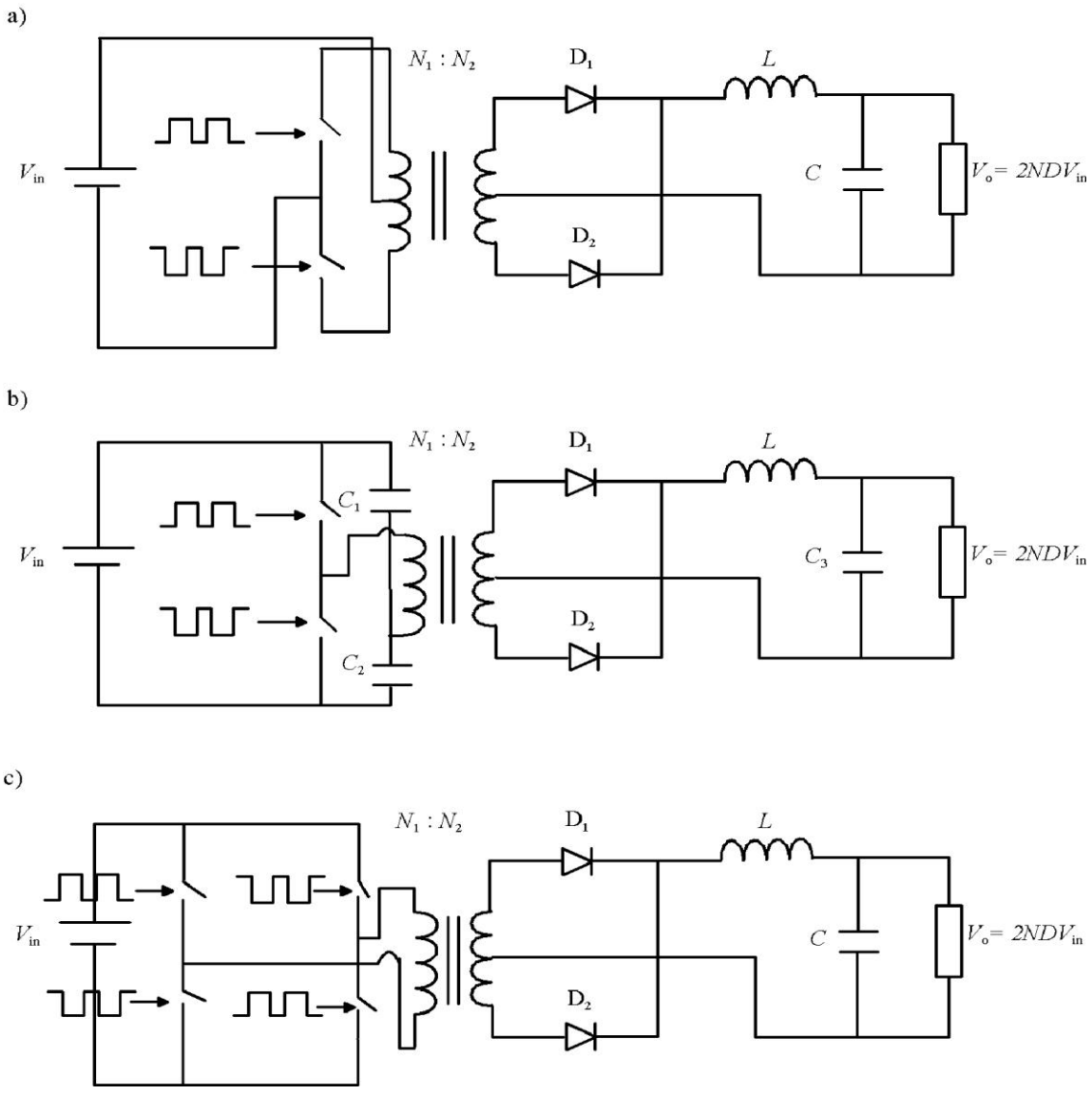


**Figure 2.6: Multiple switches topologies DC/DC converters a) Push-pull converter, b) Half-bridge converter, and c) Full-bridge**

- The Half-bridge DC/DC converter,
- The Full-bridge DC/DC converter, and
- The Push-pull DC/DC converter.

These topologies have the additional advantage over the single-ended Forward and Flyback DC-DC converters that a full flux excitation of the transformer core occurs instead of only a half core flux capability. This makes these multiple switch topologies more suited for higher power operation.

## 2.5 Controller for DC-DC Converter

In a DC-DC converter application, it is desired to obtain a constant output voltage in spite of disturbances in input voltage and load current. Therefore, the idea behind the use of negative feedback for control is to build a circuit that automatically adjusts the duty cycle as needed to obtain the desired output voltage with high accuracy, regardless of disturbances in input and load.

A block diagram of a feedback system is shown in Figure 2.7. The output voltage $v(t)$ is measured using a "sensor" with transfer function of $H(s)$ [9]. The sensor output $H(s)v(s)$ is compared with a voltage reference $V_{ref}(s)$ . The error between $H(s)v(s)$ and $V_{ref}(s)$ is feed to compensator that amplifies error signal and makes the output voltage regulated around reference voltage. In practice, the error is usually nonzero and nonetheless small enough. A compensator gain $G_c(s)$ helps to obtain a small error and improve the stability and performance of the system. The PWM (pulse width modulator) modulator is used to generate "digital" pulse width feed into the switch of converter. The pulse width changes with the comparator output voltage $V_{c(t)}$.

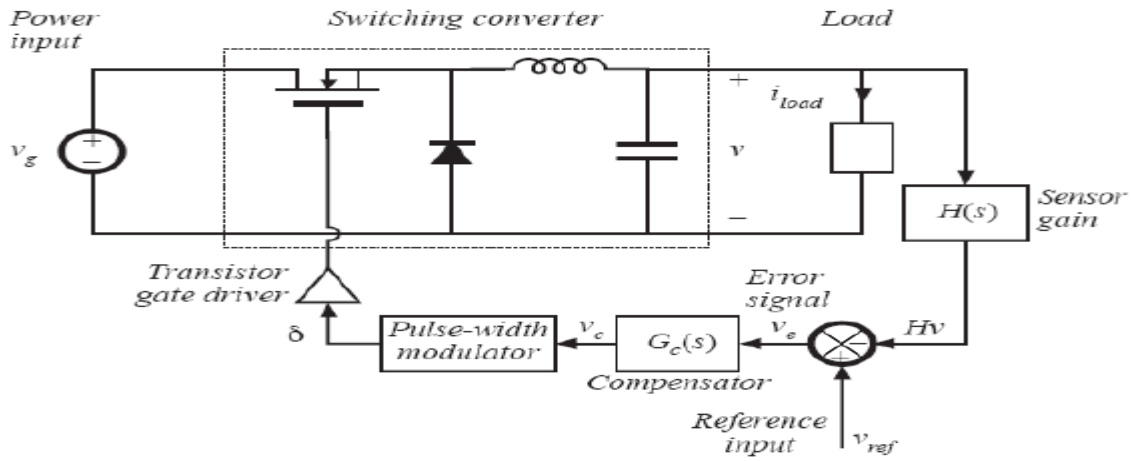


**Figure2.7 Feedback loop for switching converter**

The traditional approaches for controllers of DC-DC converters based on duty ratio adjustment have relied on analog implementation schemes. The above mentioned control strategies based on analog techniques offer robust control, but suffer from serious limitations such as sensitivity to noise and temperature change. Hence, this trend has moved towards digital control schemes, which offer multitudinous benefits. Digital controllers for switching power supplies offer a number of advantages including a reduction of the number of passive components, programmability, implementation of more advanced control algorithms and additional processing options, as well as reduced sensitivity to parameter variations.

Generally, there are several implementation approaches for digital controllers today, which include Microprocessor/DSP's (Digital Signal Processors), FPGA (Field Programmed Gates Array) and Custom IC Design. The features of these approaches are compared in the following list.

DSP:

- DSP chips can be reprogrammed;
- The speed is generally slower than ICs;
- Implementation is exceedingly complex for the intended application;
- DSP is costly over custom IC design;
- High frequency power converters have to use high performance DSPs

FPGA:

- FPGA can be programmed on site;
- The processing is faster than a general purpose DSP;
- For FPGA design there is no physical manufacturing step, which results in very short design time;
- FPGA's typical price is higher than DSPs;

Custom IC Design:

- Due to physical design consideration the typically better performance than FPGA;
- However it results in much longer design time than FPGA since there is a layout step;
- Custom IC design has lower price than FPGA and DSP.

In this thesis, the features that make DSPs effective computational engines for high frequency switching power converters are presented. A case study is introduced in which a DSP-based solution was developed as a controller for DC-DC buck converter. Which is widely used in low voltage applications. The design, implementation and testing of a DSP-based system are illustrated, and the techniques and challenges in system design based on DSPs are also addressed. DSP designs are optimized to handle real-time applications with high bandwidth requirements.

# CHAPTER 3

# MODELING ANALYSIS AND DESIGN OF BUCK CONVERTER

# 3. BUCK CONVERTER

## 3.1 States of Operation

There are two states in which the circuit given in Figure 3.1 operates. That is the ON State and the OFF State. These two states and the active circuit part for those given states are shown in the Figure 3.2 and Figure 3.3.

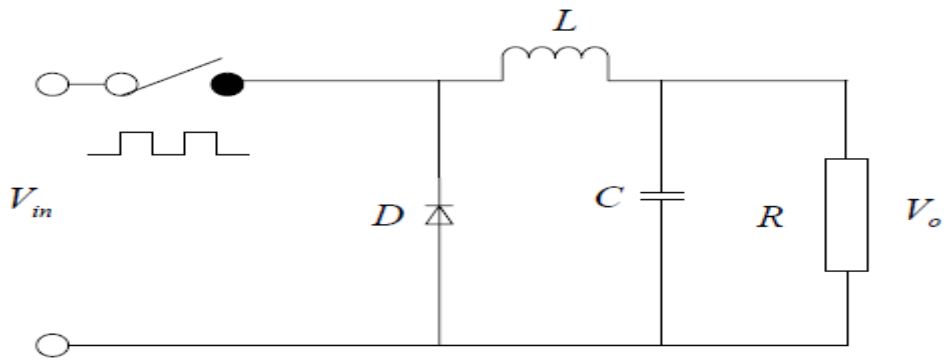


**Figure 3.1: General Buck Converter Schematic**

### 3.1.1 ON State

The operation of the buck converter is fairly simple, with an inductor and two switches (usually a transistor and a diode) that control the inductor. It alternates between connecting the inductor to source voltage to store energy in the inductor and discharging the inductor into the load.

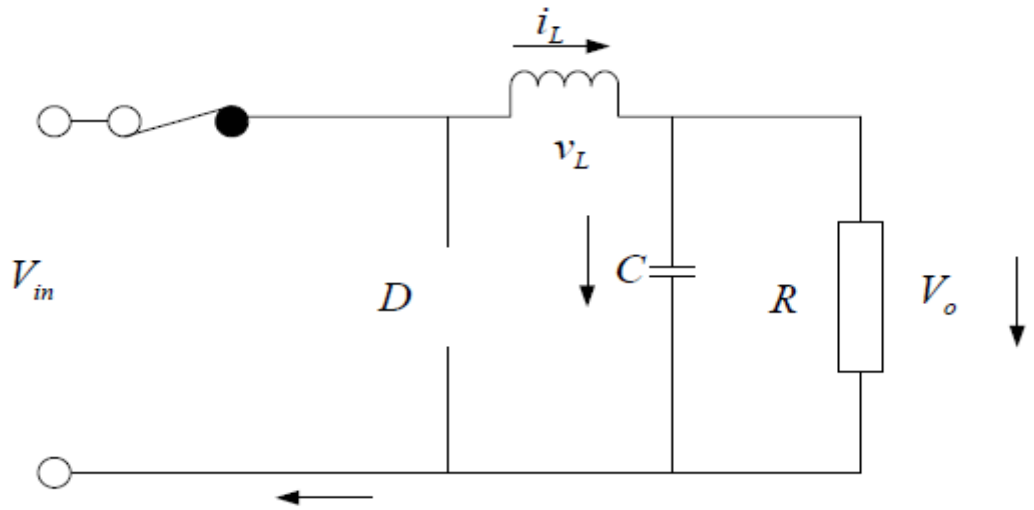


**Figure 3.2: ON State**

Refer to Figure 3.2, when the switch is connected, L is connected to the switch which tends to oppose the rising current and begins to generate an electromagnetic field in its core. Diode D is reverse biased and is essentially an open circuit at this point. The inductor current increases, inducing a positive voltage drop across the inductor and a lower output supply voltage in reference to the input source voltage. The inductor serves as a current source to the output load impedance.

### 3.1.2 OFF State

In the OFF state the switch is open, diode D conducts and energy is supplied from the magnetic field of L and electric field of C. The current through the inductor falls linearly. When the FET switch is off, the inductor current discharges, inducing a negative voltage drop across the inductor. Because one port of the inductor is tied to ground, the other port will have a higher voltage level, which is the target output supply voltage. The output capacitance acts as a low-pass filter, reducing output voltage ripple as a result of the fluctuating current through the inductor. The diode prevents the current flowing from the inductor when the FET switch is off.

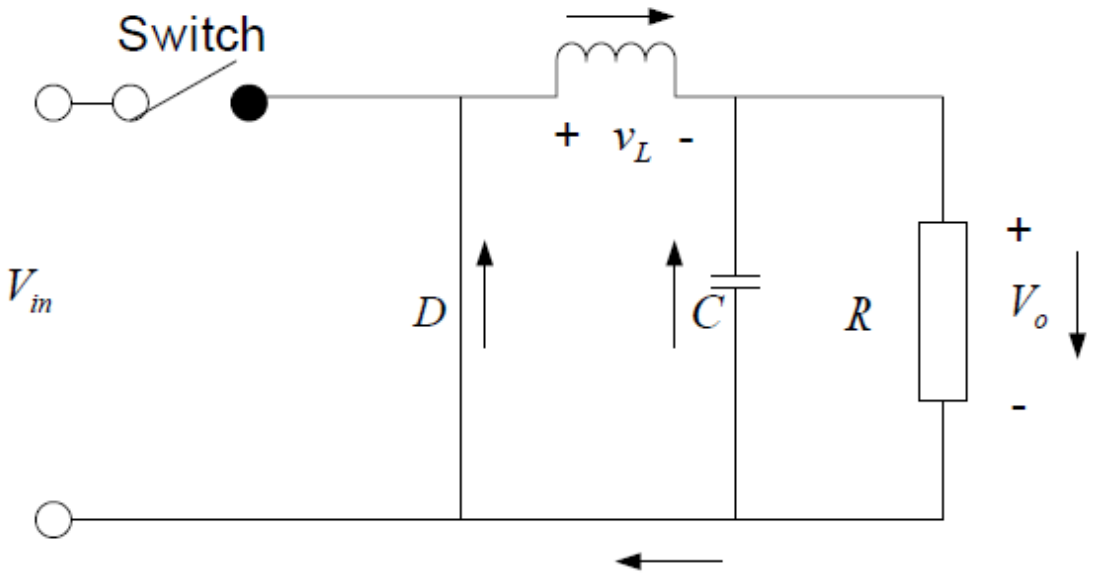


**Figure 3.3: OFF State**

## 3.3 Continuous Mode / Discontinuous Mode

During the ON state and then the subsequent OFF state the Buck Converter can operate in Continuous Mode or Discontinuous Mode. The difference between the two is that in CCM the current in the inductor does not fall to zero. See Figure 3.4

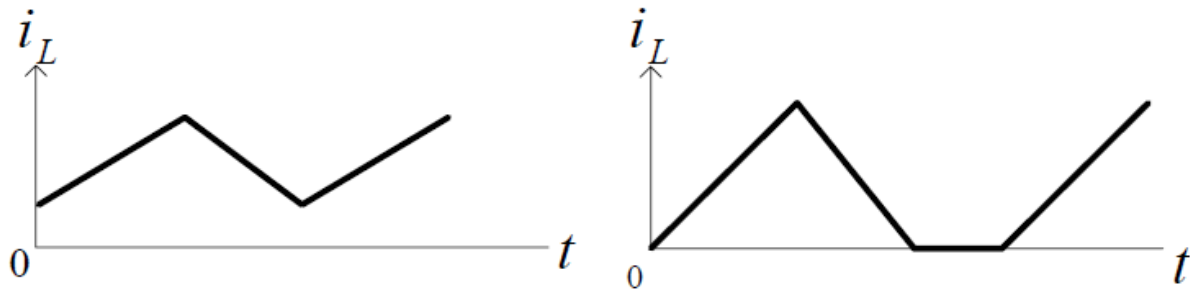


**Figure 3.4: (a) Continuous Mode (b) Discontinuous Mode**

Current flows continuously in the inductor during the entire switching cycle in steady state operation. In most Buck regulator applications, the inductor current never drops to zero during full-load operation. Overall performance is usually better using continuous mode, and it allows maximum output power to be obtained from a given input voltage and switch current rating. Energy from the battery is supplying the load and is being stored in the inductor L as a magnetic field. The current through the inductor is rising linearly.

In the DCM the current in the inductor falls to zero and remains at zero for some portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. In applications where the maximum load current is fairly low, it can be advantageous to design for discontinuous mode operation. In these cases, operating in discontinuous mode can result in a smaller overall converter size (because a smaller inductor can be used). Often the output capacitor must be large to keep the voltage constant.

## 3.4 Calculation for Duty Ratio

For calculation of the duty ratio we will first of all assume that the converter is in steady state. The switches are treated as being ideal, and the losses in the inductive and the capacitive

elements are neglected. Also it is important to point out that the following analysis does not include any parasitic resistances (all ideal case). The analysis also has the assumption that the converter is operating in Continuous conduction mode only i.e. $i_L(t) > 0$.

When the switch is on for time duration $t_{on}$ , the switch conducts the inductor current and the diode becomes reverse biased. This results in a positive voltage $v_L = V_d - V_o$ across the inductor in Figure 3.5(a). This voltage causes a linear increase in the inductor current $i_L$. When the switch is turned off, because of the inductive energy storage, $i_L$ continues to flow. This current now flows through the diode, and $v_L = -V_o$ in Figure 3.5(b).

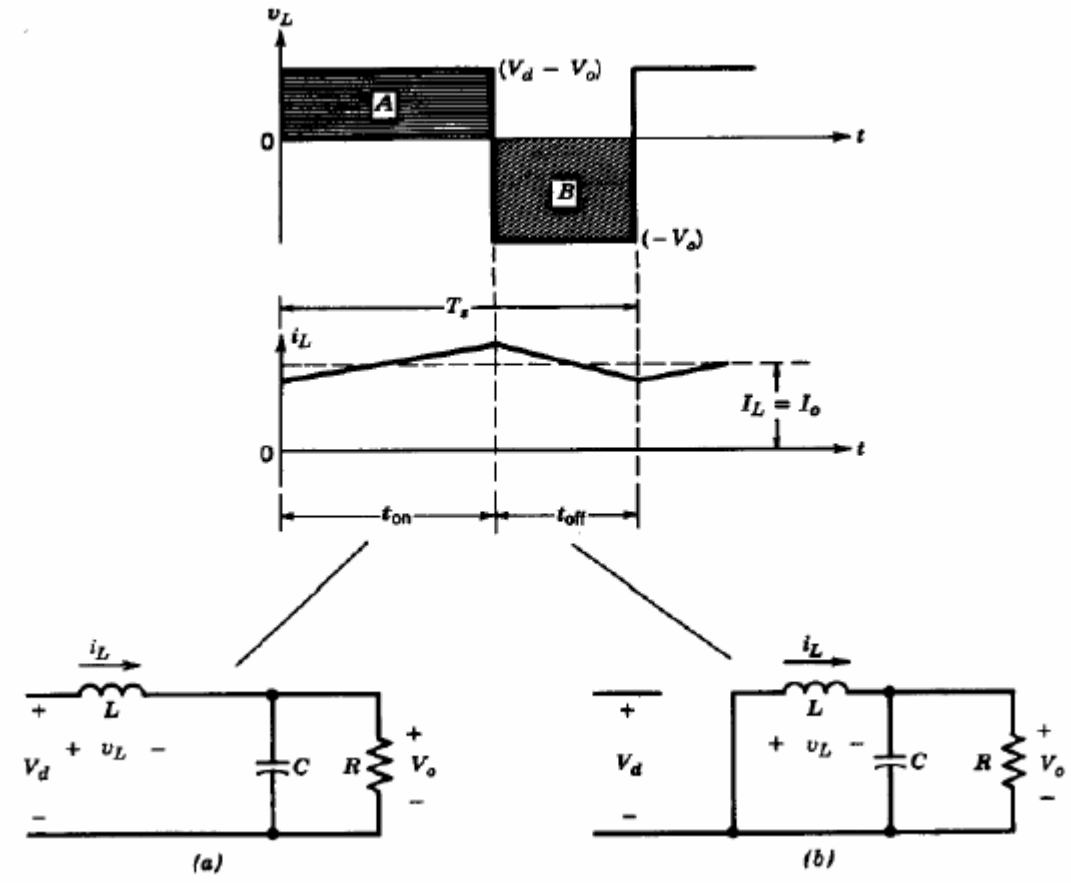


**Figure 3.5: Step-down converter circuit states: (a) switch on; (b) switch off**

Since in steady-state operation waveform must repeat from one time period to the next, the integral of the inductor voltage $v_L$ over one time period must be zero, where $T_s = t_{on} + t_{off}$ :

$$\int_0^{T_S} V_L\,dt = \int_0^{t_{on}} V_L\,dt + \int_{t_{on}}^{T_S} V_L dt = 0 \qquad (3-1)$$

From Figure 3.5, it implies that areas A and B must be equal. Therefore,

$$(V_d - V_o)t_{on} = V_o(T_s - t_{on}) \qquad (3-2)$$

or

$$\frac{V_o}{V_d} = \frac{t_{on}}{T_s} = D \qquad (3-3)$$

Hence in this mode, the voltage output varies linearly with the duty ratio of the switch for a given input voltage and does not depend on any other circuit parameter.

## 3.5 Calculation for Inductor

From Figure 3.5(a) we can derive a simplified differential equation based on the assumption that the voltage across the load, and thereby across the capacitor, is fairly constant. The differential equation in terms of the current through the inductor, when the switch is closed, may now be written as

$$L\frac{di_L(t)}{dt} = V_d - V_o \qquad (3-4)$$

Assuming that the circuit has assumed steady state hence there may already be some current in the inductor, $\boldsymbol{I_{l,min}}$, just prior to the closing of switch S. Hence for a time interval $0 \le t \le T_{ON} = DT$ , gives:

$$i_L(t) = \frac{V_d - V_o}{L}t + I_{L,min} \qquad (3-5)$$

The inductor current increases linearly with time and attains its maximum value $I_{L,\max}$ as $t \to T_{ON} = DT$ such that

$$I_{L,max} = \frac{V_d - V_o}{L}DT + I_{L,min} \qquad (3-6)$$

Defining the change in the current from its minimum to maximum value as the peak-to-peak current ripple $I_L$ , the equation 3-6 yields an expression for $I_L$ ,as in Eq. 3-7.

$$\Delta I_L = I_{l,max} - I_{L,min} = \frac{V_d - V_o}{L} DT \qquad (3-7)$$

Note that the current ripple is directly proportional to D, the duty cycle, upon which we may not have any control because of the output voltage requirement. However, it is inversely proportional to the inductance L upon which we can exert some controls. Thus, the current ripple can be controlled by a proper selection of the inductor.

Let us now analyze the circuit when the switch is in its open position. The inductor current completes its path through the lower side MOSFET and the corresponding differential equation, for $0 \leq t \leq T_{OFF}$ , is given by Eq. 3-8.

$$L \frac{di_L(t)}{dt} = -V_o \qquad (3-8)$$

From the solution of the above first-order differential equation, we obtain

$$i_L(t) = -\frac{V_o}{L} t + I_{L,max} \qquad (3-9)$$

Where $I_{L,\max}$ is the maximum value of the current in the inductor at the opening of the switch or the beginning of the off period. *As* $t \rightarrow T_{off}$ *= (1-D) T,* the inductor current decreases to its minimum value $i_{L,min}$ such that.

$$i_{L,min}(t) = -\frac{V_o}{L}(1-D)T + I_{L,max} \qquad (3-10)$$

The Eq. 3-10 yields another expression for the peak-to-peak current ripple as given in Eq. 3-11

$$\Delta I_L = I_{l,max} - I_{L,min} = -\frac{V_o}{L}(1-D)T \qquad (3-11)$$

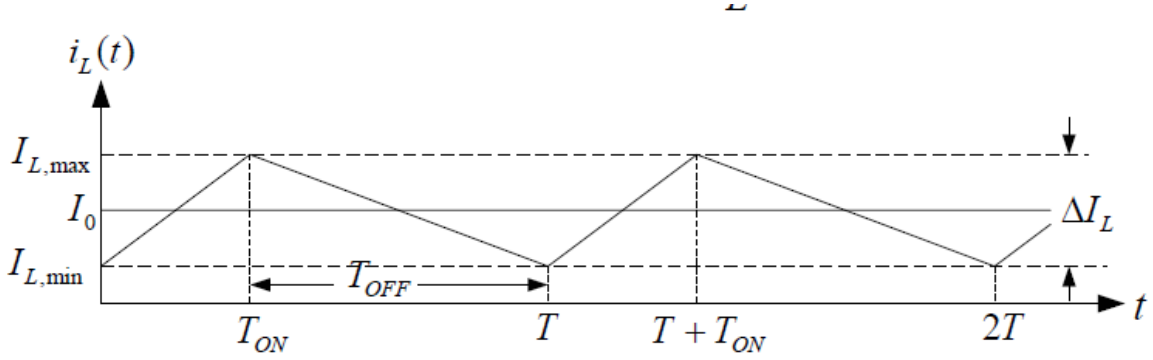


**Figure 3.6: Inductor Current**

The current through the inductor as given by Eq. 3-5 during the on time and by Eq. 3-9 during the off time is sketched in the Figure 3.6. The average current in the inductor must be equal to the dc current through the load. That is,

$$I_{L,avg} = I_o = \frac{V_o}{R} \qquad (3-12)$$

The expressions for the maximum and minimum currents through the inductor may now be written as

$$I_{l,max} = I_{L,avg} + \frac{\Delta I_L}{2} = \frac{V_o}{R} + \frac{V_o}{2L}(1-D)T \qquad (3-13)$$

$$I_{l,min} = I_{L,avg} - \frac{\Delta I_L}{2} = \frac{V_o}{R} - \frac{V_o}{2L}(1-D)T \qquad (3-14)$$

The current supplied by the source varies from $I_{L,\min}$ to $I_{L,\max}$ during the time the switch is closed and is zero otherwise as shown in Figure 3.7.

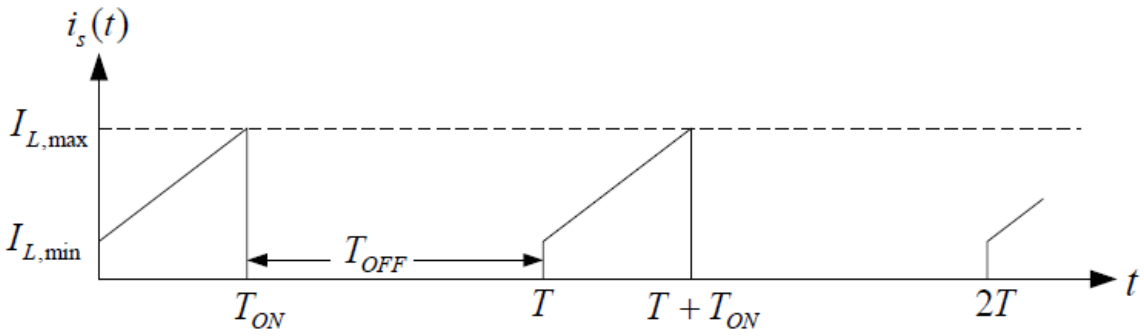


**Figure 3.7: The source current**

When the switch, the inductor, and the capacitor are treated as ideal elements, the average power dissipated by them is zero. Consequently, the average power supplied by the source must be equal to the average power delivered to the load. That is,

$$V_d I_d = V_o I_o = D V_s I_o \qquad (3-15)$$

This equation helps us express the average source current in terms of the average load current as given in Eq. 3-16.

$$I_s = D I_o \qquad (3-16)$$

The current through the lower side MOSFET is shown in Figure 3.8. Its average value is given by Eq. 3-17.

$$I_{LS} = (1-D) I_o \qquad (3-17)$$

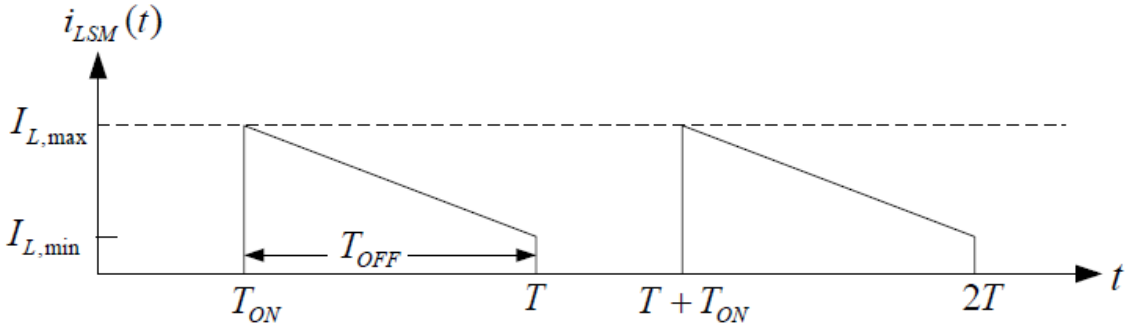


**Figure 3.8: Current through the low side MOSFET**

We know the fact that the buck converter can either operate in its continuous conduction mode or discontinuous mode. When it operates in the continuous conduction mode, there is always a current in the inductor. The minimum current in the continuous conduction mode can be zero. Consequently, there is a minimum value of the inductor that ensures its continuous conduction mode. It can be obtained from Eq. 3-14 by setting $I_{L,\min}$ to zero as

$$\frac{V_o}{R} - \frac{V_o}{2L_{min}}(1-D)T = 0 \qquad (3-18)$$

Hence,

$$L_{min} = \frac{1-D}{2}RT = \frac{1-D}{2f}R \qquad (3-19)$$

## 3.6 Calculation for Capacitor

The output capacitor is assumed to be so large as to yield $v_o(t) = V_o$ . However, the ripple in the output voltage with a practical value of capacitance can be calculated by considering the waveforms shown in Figure 3.9 for a continuous-conduction mode of operation. Assuming that the entire ripple component in $i_L$ flows through the capacitor and its average component flows through the load resistor, the shaded area in Figure 3.9 represents an additional charge ΔQ.

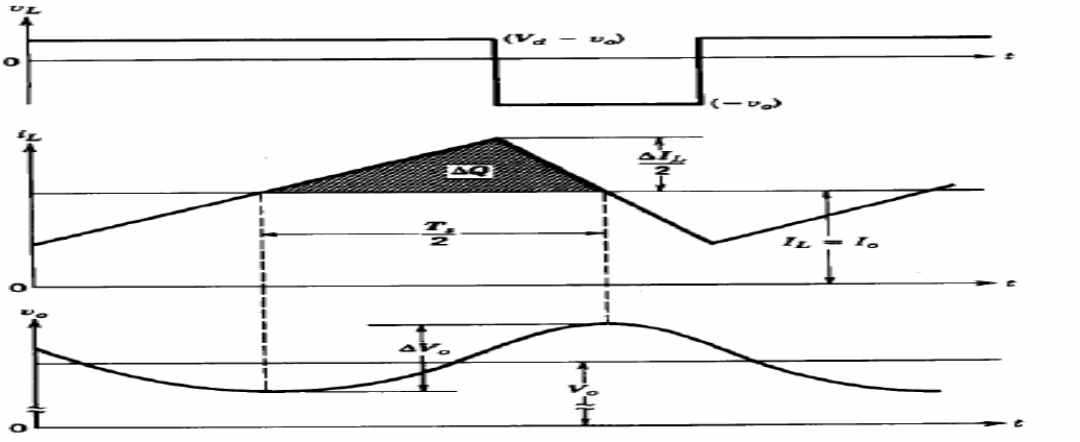


**Figure 3.9: Output voltage ripple in a step-down converter**

Therefore, the peak to peak voltage ripple $\Delta V_o$ can be written as

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{\Delta I_L T_s}{8C} \qquad (3-20)$$

From Figure 3.9 during $t_{off}$

$$\Delta I_L = -\frac{V_o}{L}(1-D)T_s \qquad (3-21)$$

Therefore, substituting $\Delta I_L$ from Eq. 3-21 into the Eq. 3-20 gives

$$\Delta V_o = \frac{T_s}{8C}\frac{V_o}{L}(1-D)T_s \qquad (3-22)$$

$$\frac{\Delta V_o}{V_o} = \frac{T_s^2}{8LC}(1-D)T_s = \frac{\pi^2}{2}(1-D)\left(\frac{f_c}{f_s}\right)^2 \qquad (3-23)$$

Where switching frequency $f_s = 1/T_s$ and

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad (3-24)$$

Equation 3-23 shows that the voltage ripple can be minimized by selecting a corner frequency $f_c$ of the low pass filter at the output such that $f_c << f_s$. Also, the ripple is independent of the output load power, so long as the converter operates in the continuous-conduction mode. We should note that in switch-mode dc power supplies, the percentage ripple in the output voltage are usually specified to be less than, for instance, 1%.

The analysis carried out above assumes ideal components and if we were to make the analysis using all the non-ideal components it would make the derivation a bit more complex with a lot of other parameters included in the final equation. But for the calculation of initial values of the components the above approximations does result in reasonable values. It is also important to realize here that the ESR and ESL are also important and can even dominate. More about how the non-ideality can affect the overall system can be found on [21].

## 3.7 Linearization using State-Space Averaging

The goal of the following analysis is to obtain a small signal transfer function $\tilde{V}_o(s)/\tilde{d}(s)$ where $\tilde{V}_o(s)$ and $\tilde{d}(s)$ are small perturbations in the output voltage $V_o$ and the switch duty ratio $d$, respectively, around their steady-state dc operating values $V_o$ and D.

### 3.7.1 Power Stage & Output Filter

**Step 1 State-Variable Description for Each Circuit State.** In a converter operating in a continuous-conduction mode, there are two circuit states: one state corresponds to when the switch is on and the other to when the switch is off. A third circuit state exists during the discontinuous interval, which is not considered in the following analysis because of the assumption of a continuous-conduction mode of operation.

During each circuit state, the linear circuit is described by means of the state-variable vector **x** consisting of the inductor current and the capacitor voltage. In the circuit description, the parasitic elements such as the resistance of the filter inductor and the equivalent series resistance (ESR) of the filter capacitor should also be included. Here $V_d$ is the input voltage. A lowercase letter is used to represent a variable, which includes its steady-state dc value plus a small ac perturbation, for example, $v_o=V_o+\tilde{V}_o$ Therefore, during each circuit state, we can write the following state equations:

$$\dot{X} = A_1X + B_1V_d \quad during\ d.T_s \qquad (3-26)$$

and

$$\dot{X} = A_2X + B_2V_d \quad during\ (1-d).T_s \qquad (3-27)$$

Where $\mathbf{A}_1$ and $\mathbf{A}_2$ are state matrices and $\mathbf{B}_1$ and $\mathbf{B}_2$ are vectors.

The output $v_o$ in all converters can be described in terms of their state variables alone as

$$v_o = C_1X \quad during\ d.T_s \qquad (3-28)$$

and

$$v_o = C_2 X \quad during\ (1-d).T_s \qquad (3-29)$$

Where $\mathbf{C}_1$ and $\mathbf{C}_2$ are transposed vectors.

**Step 2: Averaging the State-Variable Description Using the Duty Ratio *d*.** To produce an average description of the circuit over a switching period, the equations corresponding to the two foregoing states are time weighted and averaged, resulting in the following equations:

$$\dot{X} = [A_1 d + A_2]X + [B_1 + B_2(1-d)]V_d \quad (3-30)$$

and

$$v_o = [C_1 d + C_2(1-d)]X \qquad (3-31)$$

**Step 3: Introducing Small ac Perturbations and Separation into ac and dc Components.** Small ac perturbations, represented by "~", are introduced in the dc steady-state quantities (which are represented by the upper case letters). Therefore,

$$x = X + \tilde{x} \qquad (3-32)$$

$$v_o = V_o + \tilde{v_o} \qquad (3-33)$$

and

$$d = D + \tilde{d} \qquad (3-34)$$

In general, $v_d = V_d + \tilde{v_d}$. However, in view of our goal to obtain the transfer function between voltage $\tilde{v_o}$ and the duty ratio $\tilde{d}$ , the perturbation $\tilde{v_d}$ is assumed to be zero in the input voltage to simplify our analysis. Therefore

$$v_d = V_d \qquad (3-35)$$

Using Eq. 3-32 through 3-35 in Eq 3-30 and recognizing that in steady state, $\dot{\mathbf{X}} = 0$,

$\dot{\tilde{x}} = AX + BV_d + A\tilde{x} + [(A_1 - A_2)X + (B_1 - B_2)V_d]\tilde{d}$ +terms containing products of $\tilde{x}$ and $\tilde{d}$ to be neglected $(3-36)$

Where

$$A = A_1 D + A_2(1-D) \qquad (3-37)$$

and

$$B = B_1 D + B_2(1-D) \qquad (3-38)$$

The steady-state equation can be obtained from Eq. 3-36 by setting all the perturbation terms and their derivatives to zero. Therefore, the steady-state equation is

$$AX + BV_d = 0 \qquad (3-39)$$

and therefore in Eq. 3-36

$$\dot{\tilde{x}} = A\tilde{x} + [(A_1 - A_2)X + (B_1 - B_2)V_d]\tilde{d} \qquad (3-40)$$

Similarly, using Eq. 3-32 to 3-34 in Eq. 3-31 results in

$$V_o + \widetilde{v_o} = CX + C\tilde{x} + [(C_1 - C_2)X]\tilde{d} \qquad (3-41)$$

where

$$C = C_1 D + C_2(1-D) \qquad (3-42)$$

In Eq. 3-41, the steady-state output voltage is given as

$$V_o = CX \qquad (3-43)$$

and therefore,

$$\widetilde{v_o} = C\tilde{x} + [(C_1 - C_2)X]\tilde{d} \qquad (3-44)$$

Using Eq. 3-39 and 3-43, the steady-state dc voltage transfer function is

$$\frac{V_o}{V_d} = CA^{-1}B \qquad (3-45)$$

**Step 4: Transformation of the ac Equations in to *s*-Domain to Solve for the Transfer Function.** Equations 3-40 and 3-44 consist of the ac perturbations. Using Laplace transformation

in Eq. 3-40.

$$S\widetilde{x(s)} = A\widetilde{x(s)} + [(A_1 - A_2)X + (B_1 - B_2)V_d]\widetilde{d(s)} \qquad (3-46)$$

or

$$\widetilde{x(s)} = [SI - A]^{-1} + [(A_1 - A_2)X + (B_1 - B_2)V_d]\widetilde{d(s)} \qquad (3-47)$$

Where **I** is the unity matrix. Using a Laplace transformation in Eq. 3-44 and expressing in terms $\widetilde{x(s)}$ in terms of $\widetilde{d(s)}$ from Eq. 3-47 results in the desired transfer function $T_p(s)$ of the power stages:

$$T_p(s) = \frac{\widetilde{v_o(s)}}{\widetilde{d(s)}} = C[SI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X \qquad (3-48)$$

### 3.7.2 Buck Converter

Now we will linearize the power stage and the output filter of the Buck Converter given in Figure 3.15. The two switches are represented by diodes.

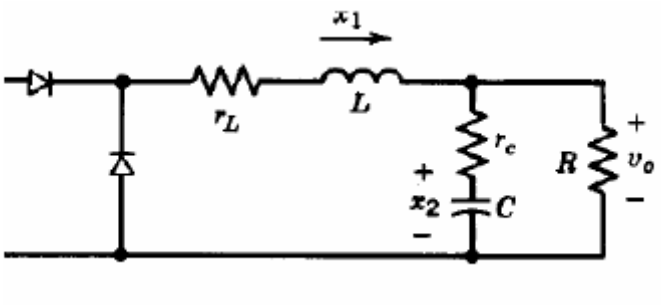


**Figure 3.15: Buck Converter Circuit**

$r_L$ is inductor resistance, $r_c$ is the equivalent series resistance of the capacitor, and R is the load resistance.

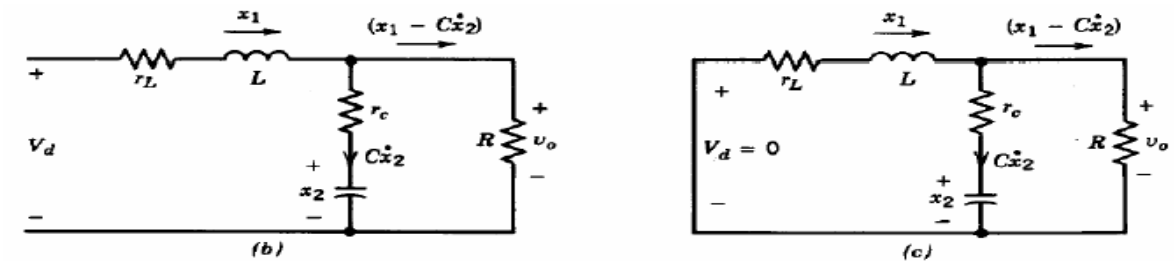


**Figure 3.16: Buck Converter (a) switch on; (b) switch off**

From Figure 3.16 the following equations can be derived.

$$-V_d + L\dot{x}_1 + r_L x_1 + R(x_1 - C\dot{x}_2) = 0 \qquad (3-49)$$

and

$$-x_2 - Cr_c\dot{x}_2 + R(x_1 - C\dot{x}_2) = 0 \qquad (3-50)$$

In matrix form, these two equations can be written as

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix} -\dfrac{Rr_c + Rr_L + r_C r_L}{L(R+r_C)} & -\dfrac{R}{L(R+r_C)} \\ \dfrac{R}{C(R+r_C)} & -\dfrac{1}{C(R+r_C)} \end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix} V_d \qquad (3-51)$$

Comparing the equations with Eq. 3-26 yields

$$A_1 = \begin{bmatrix} -\dfrac{Rr_c + Rr_L + r_C r_L}{L(R+r_C)} & -\dfrac{R}{L(R+r_C)} \\ \dfrac{R}{C(R+r_C)} & -\dfrac{1}{C(R+r_C)} \end{bmatrix} \qquad (3-52)$$

and

$$B_1 = \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix} \qquad (3-53)$$

The state equation for the circuit of Fig 3.15 with the switch off can be written by observation, noting that the circuit of Fig. 3.16(b) is exactly the same as the circuit of Fig 3.16(a) with $V_d$ set to zero.

$$A_2 = A_1 \qquad (3-54)$$

$$B_2 = 0 \qquad (3-55)$$

The output voltage in both the circuit states is given as

$$v_o = R(x_1 - C\dot{x}_2) \qquad (3-56)$$

$$= \frac{Rr_C}{R+r_C}x_1 + \frac{R}{R+r_C}x_2$$

Using $\dot{x}_2$ from Eq. 3-50

$$= \begin{bmatrix} \frac{Rr_c}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

Therefore, in Eq. 3-28 and 3-29

$$C_1 = C_2 = \begin{bmatrix} \frac{Rr_c}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix} \quad (3-57)$$

$$A = A_1 \quad (from\ Eq-37\ and\ Eq-54) \quad (3-58)$$

$$B = B_1 D \quad (from\ Eq-38\ and\ Eq-55) \quad (3-59)$$

$$C = C_1 \quad (from\ Eq-42\ and\ Eq-57) \quad (3-60)$$

*Model Simplification:* In all practical circuits,

$$R \gg (r_C + r_L) \quad (3-61)$$

Therefore, **A** and **C** are simplified as:

$$A = A_1 = A_2 = \begin{bmatrix} -\frac{r_C + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad (3-62)$$

$$C = C_1 = C_2 = [r_C \quad 1] \quad (3-63)$$

and **B** remains unaffected as:

$$B = B_1 D = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} D \quad (3-64)$$

Where $\mathbf{B}_2$=0. From Eq. 3-62,

$$A^{-1} = \frac{LC}{1 + (r_C + r_L)/R} \begin{bmatrix} -\frac{1}{RC} & \frac{1}{L} \\ -\frac{1}{C} & -\frac{r_C + r_L}{L} \end{bmatrix} \quad (3-65)$$

$$\frac{V_o}{V_d} = D \frac{R + r_C}{R + (r_C + r_L)} \cong D \quad (3-66)$$

$$T_p(s) = \frac{\widetilde{v_o(s)}}{\widetilde{d(s)}} \cong V_d \frac{1 + Sr_C C}{LC[S^2 + S\left\{\frac{1}{RC} + \frac{(r_C + r_L)}{L}\right\} + \frac{1}{LC}]} \qquad (3-67)$$

Eq. 3-67 is the Open Loop Transfer Function of the circuit represented in Figure 3.16. The term in the third brackets in the denominator of Eq. 3-69 are of the form $S^2 + 2\varepsilon\omega_o S + \omega_o^2$, where

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad (3-68)$$

$$\varepsilon = \frac{\frac{1}{RC} + \frac{r_C + r_L}{L}}{2\omega_o} \qquad (3-69)$$

Therefore, from Eq. 3-67 the transfer function can be written as

$$T_p(s) = \frac{\widetilde{v_o(s)}}{\widetilde{d(s)}} = V_d \frac{\omega_o^2}{\omega_z} \frac{S + \omega_z}{S^2 + \varepsilon\omega_o S + \omega_o^2} \qquad (3-70)$$

Where a zero is introduced due to the equivalent series resistance of the output capacitor at the frequency

$$\omega_z = F_{ESR} = \frac{1}{r_C C} \qquad (3-71)$$

## 3.8 Design Parameters

The converter, in this thesis, is designed for CCM operation, and needs to operate from a 12 ± 3 V DC source. The output voltage, $V_o$, from the converter must be 2 ± 0.1 V with a steady-state ripple of less than 2.5 percent or 0.05 V. The converter is required to maintain output voltage while the output current, $I_o$, varies between 1 A and 10 A.

## 3.9 Time-Domain Analysis of Open-Loop Buck Converter

The time-domain response of the buck converter needs to maintain within operating parameters stated within section 3.8. As the input source varies ±3 V and loads vary between 1 A and 10 A, the output voltage is required to be 2 ± 0.1 V. Three separate responses are analyzed to see if the buck converter remains within the required operating parameters: connection to the 12 V DC power source, 1 A step change in the load, and 1 V step change in the power source.

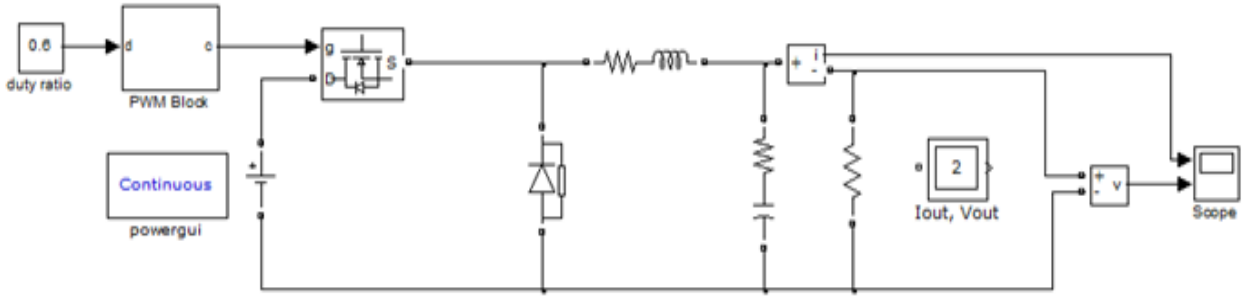


**Figure 3.17: Simulink model of buck converter**

### 3.9.1 Response to 12 V DC Power Source

The buck circuit is required to reach a steady-state voltage of 2 V when connected to a 12 V power source. The converter is connected to the source operating under minimum loading conditions: 1 A. The duty cycle is set to 0.2891. From the response shown in Figure 3.18, it can be seen that the output voltage meets the steady-state op-rating conditions; the steady-state error is 0.4 percent. The transient characteristics are a maximum overshoot of 69.4 percent, a rise time of 88 sec, and a settling time of 2.75 msec.

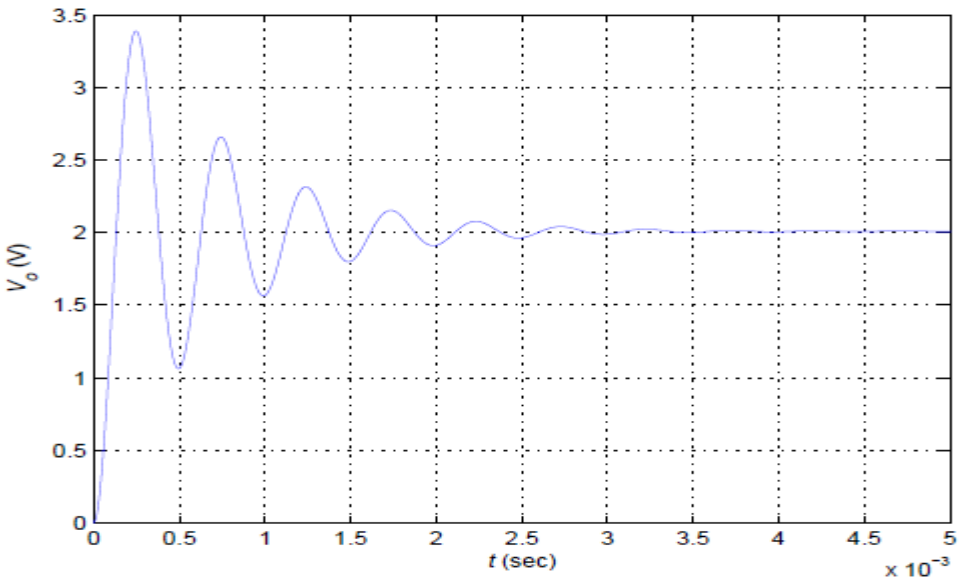


**Figure 3.18: Uncompensated open-loop time-response of buck converter to a 12 V power source with a duty cycle of 0.2891.**

### 3.9.2 Response to 1 A Step Change in Load Current

The load is capable of varying between 1 A and 10 A after the system has reached steady-state. The changes in the load alter the operating condition of the system and therefore changes in the load are analyzed to see if the system still remains within operating parameters after a change in the load has occurred. To test the system, a 1 A step change in the load is applied. The response can be seen in Figure 3.19. The output voltage response still meets steady-state operating conditions but the transient operating parameters are not satisfied. The steady-state error is 1 percent. The maximum overshoot is 7.5 percent, and the maximum undershoot is 13.5 percent, which exceed outside the 5 percent requirement.

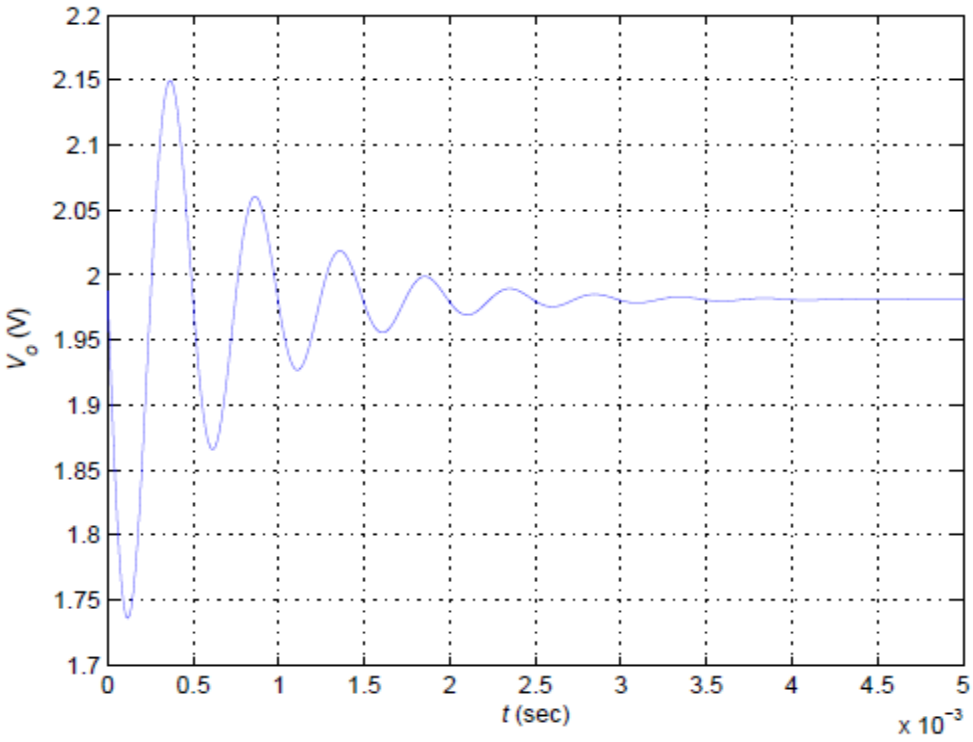


**Figure 3.19: Uncompensated open-loop time-response to a 1 A step change in the load current with a duty cycle of 0.2891.**

### 3.9.3 Response to 1 V Step Change in Power Source

The source is capable of varying ±3 V, and changes in the source voltage affect the operating condition of the system, and therefore can impact the output voltage. To test if the system

remains within operating parameters, a 1 V step change is applied to the converter after response from the power source has reached steady-state. The response of the output voltage can be seen in Figure 3.20. The output voltage no longer meets the steady-state operating requirements. The steady-state error is 8.4 percent. In addition, the peak response of the system is 2.282 V, which exceeds the 5 percent requirement.

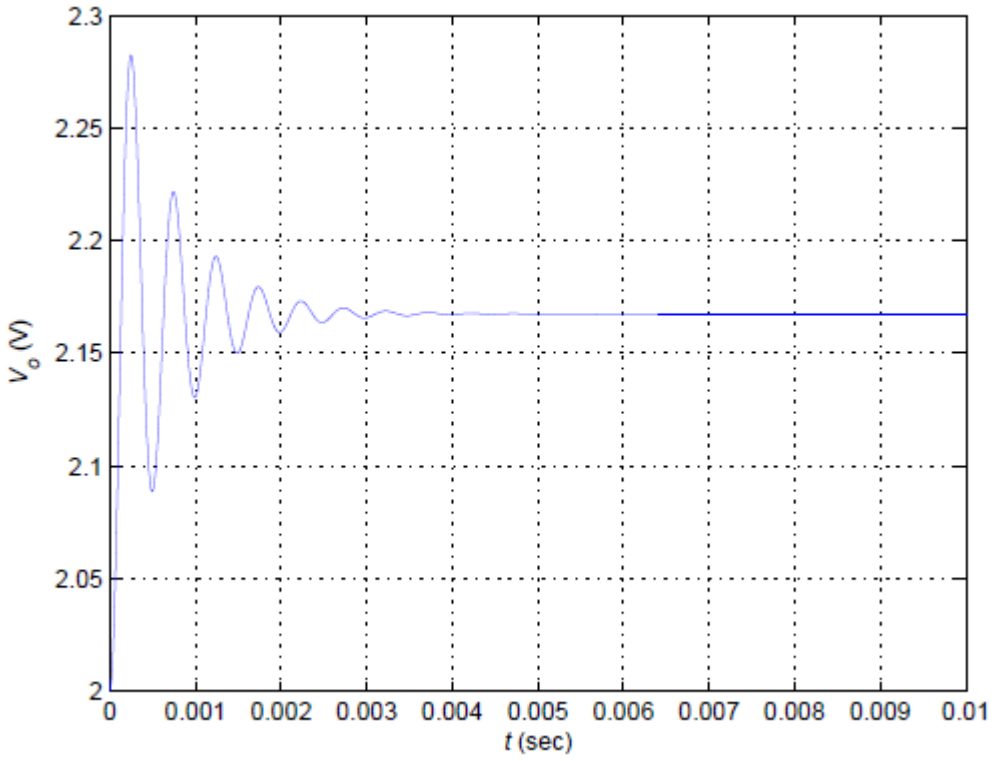


**Figure 3.20: Uncompensated open-loop time-response to a 1 V step change in source voltage with a duty cycle of 0.2891**

# CHAPTER 4

# ANALOG AND DIGITAL DESIGN OF PID CONTROLLER

# 4. Introduction

In this chapter, typical methods used to design analog and digital PID controllers are discussed. First, PID compensator design based upon root locus is introduced, and the procedure for designing the compensator is explained. Next, PID design based on a frequency response method is discussed.

## 4.1 Analog PID

Analog PID controllers are common in many applications. They can be easily constructed using analog devices such as operational amplifiers, capacitors and resistors. They are reliable in mechanical feedback systems, and able to satisfy many control problems.

### 4.1.1 Root Locus Method

Root locus is one of the methods used to design control systems. It is a technique that plots closed-loop poles in the complex plane as the gain varies from zero to infinity. It is a method that analyses the relationship between the poles, gain and the stability of the system. By understanding the root locus plot, one can design a controller to novel specifications, and understand clearly how different controller architectures affect the system.

In a root locus, the imaginary component of a pole corresponds to damped natural frequency, while the radius from the origin to the pole corresponds to natural frequency. The settling time for a system is determined by the slowest response among all responses. The least settling time can be achieved if the roots fall to the far left on the left-hand plane; overshoot can be prevented by placing the poles on the real axis.

In order to design a PID controller using the root locus method, the system must be first transformed into a transfer function. In general, root locus technique analyzes only single input single output (SISO) systems. However, an appropriate approximation of transforming a multi input multi output (MIMO) system into a SISO model can produce a close estimation of the characteristics of the system. A root locus that passes through the right-hand plane is considered unstable, whereas one that remains in the left-hand plane implies a stable system. A root locus

that falls in the jω axis (between the right- and left-hand planes) is considered marginal stable.

Figure 4.1 is an example of a close loop system. K represents the PID controller, G represents the transfer function of the system, and H represents the feedback parameter.

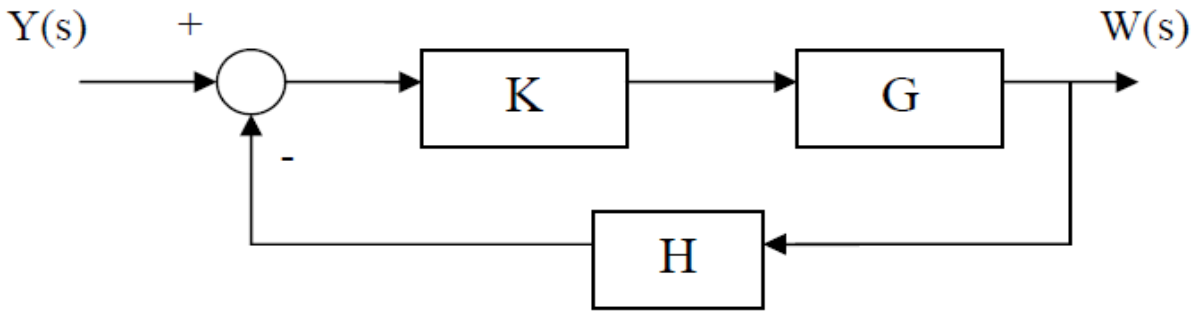


**Figure 4.1: Closed loop system**

#### 4.1.1.1 Procedures for Designing an Analog PID Controller by the Root Locus Method

1. Develop a set of reasonable transient specification based upon the particular application. From the specifications, find a pair of closed-loop dominant poles which meet these specifications, $s_1$ and $s_1$*.
2. Find $K_I$ term from steady-state error, $e_{ss}$.
3. Lump $\frac{K_I}{S}$ term into the $G_{PID}$ together with G(S).
4. Solve for $K_P$ and $K_D$ by using

$$G_{PID}G(s_1) = -1 \qquad (4\text{-}1)$$

Equation 4-1 is rearranged such that

$$K_P + K_D s_1 = -\frac{1}{G(s_1)} - \frac{K_I}{s_1} \qquad (4\text{-}2)$$

5. Hence, $K_P$ and $K_D$ can be solved by equating the real and imaginary term on the left and right side of the equation.
6. Ketch the resulting root locus for the compensated system

#### 4.1.1.2 PID Controller Design for Buck Converter

A PID controller is designed for the control of buck converter using the following specification and the transfer function of the buck converter derived in section 3.7.2.

- Settling time < 0.137 second
- Overshoot < 30%
- Steady state error = 0

$$G(s) = \frac{\widetilde{v_o(s)}}{\widetilde{d(s)}} \cong V_d \frac{1 + S r_C C}{LC[S^2 + S\left\{\frac{1}{RC} + \frac{(r_C + r_L)}{L}\right\} + \frac{1}{LC}]}$$

From the design specification, the desired closed-loop dominant poles are -29.14+j47.02. By going through procedure 3 to 6 in section 4.1.1.1, proportional, integral and derivative gains are found 900.12, 22507 and 9 respectively. Therefore the transfer function of the PID controller is given by

$$G_{PID}(s) = 900.12 + \frac{2250}{S} + 9S \qquad (4-3)$$

### 4.1.2 Frequency Response Method

Frequency response is another method commonly used to design a PID controller. Unlike root locus for the s-domain, using poles and zeros, frequency response uses the magnitude and phase of the controller to shape the curve in order to meet the specifications.

Each individual term of a PID controller is defined differently in Bode plots. As in root locus, the proportional term does not change the shape of the plot; it adjusts the gain and phase margins by shifting the magnitude of the Bode plot up or down. The integral term adds a slope of

-20dB/dec to the phase; it tends to destabilize the system by adding a constant -90 degrees to the phase angle of the system. The derivative term increases the phase margin by adding a +90 degree phase angle into the system, which corresponds to the damping ratio; also, a slope of +20dB/dec is contributed to the phase.

Two important parameters in determining the system stability in the frequency response method are gain margin (GM) and phase margin (PM). Phase margin can be found by finding the crossover frequency when the phase angle is -180 degrees, and measuring the magnitude distance below 0 dB. Similarly, gain margin can be found by finding the crossover frequency when the magnitude plot is 0 dB, and measuring the angle distance above -180 degrees. The system is unstable if the magnitude plot is not below the 0 dB line when the system is at -180 degrees, or if the phase plot is not above - 180 degrees when the system is at 0 dB

#### 4.1.2.1 Procedures for Designing an Analog PID Controller by the Frequency Response Method

1. Make sure the open loop system is stable.
2. Draw the Bode plot of the open loop system.
3. From the design specification, phase margin is related to damping ratio, ζ as in Eq. 4-4.Also, the ratio of the crossover frequency and the natural frequency is related as in Eq. 4-5.

$$\text{Phase Margin} = \tan^{-1}\frac{2\zeta}{\sqrt{-2\zeta^2+\sqrt{1+4\zeta^4}}} \qquad (4\text{-}4)$$

$$\frac{\omega_c}{\omega_n} = \sqrt{-2\zeta^2+\sqrt{1+4\zeta^4}} \qquad (4\text{-}5)$$

4. By understanding the contribution of P, I and D on a Bode plot, they can be specified such that the design specification for a closed loop system, such as phase margin and crossover frequency can be fulfilled.

### 4.1.2.2 PID Controller Design for Buck Converter

The Bode plot of the open loop system is shown in Figure 4.2

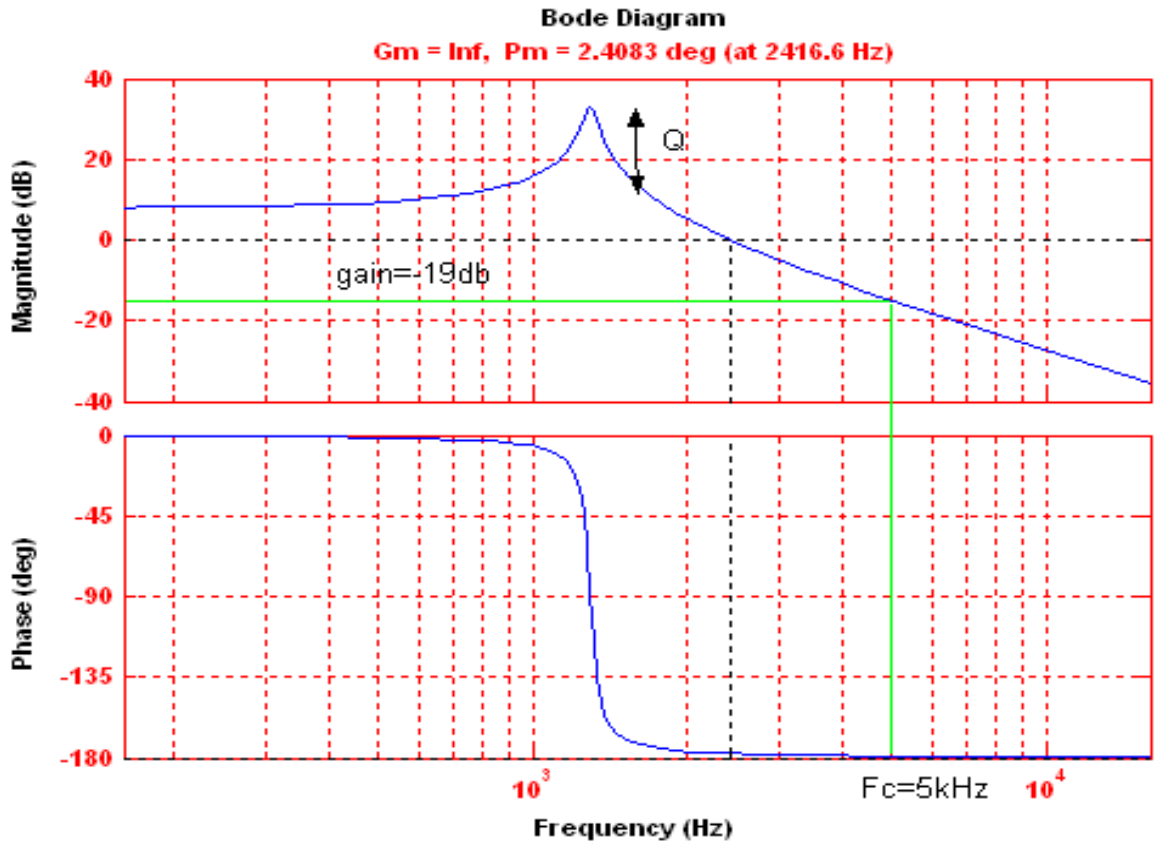


**Figure 4.2: Bode Plot of the open loop system**

From Eq. 4.4 and Eq. 4.5, the phase margin is found to be 2.4083 degree, and the crossover frequency is 2416.6Hz. Thus the P, I and D gain are 885, 22000.5 and 10 respectively. Thus the transfer function of the PID controller is given by

$$G_{PID}(s) = 885 + \frac{2200.5}{s} + 10S \qquad (4-6)$$

The Bode plot of the compensated system is shown in Figure 4.3. It should be noted that the phase margin has improved significantly. The phase margin of the compensated system is 47.5 degree, and the crossover frequency is 5282.5Hz.

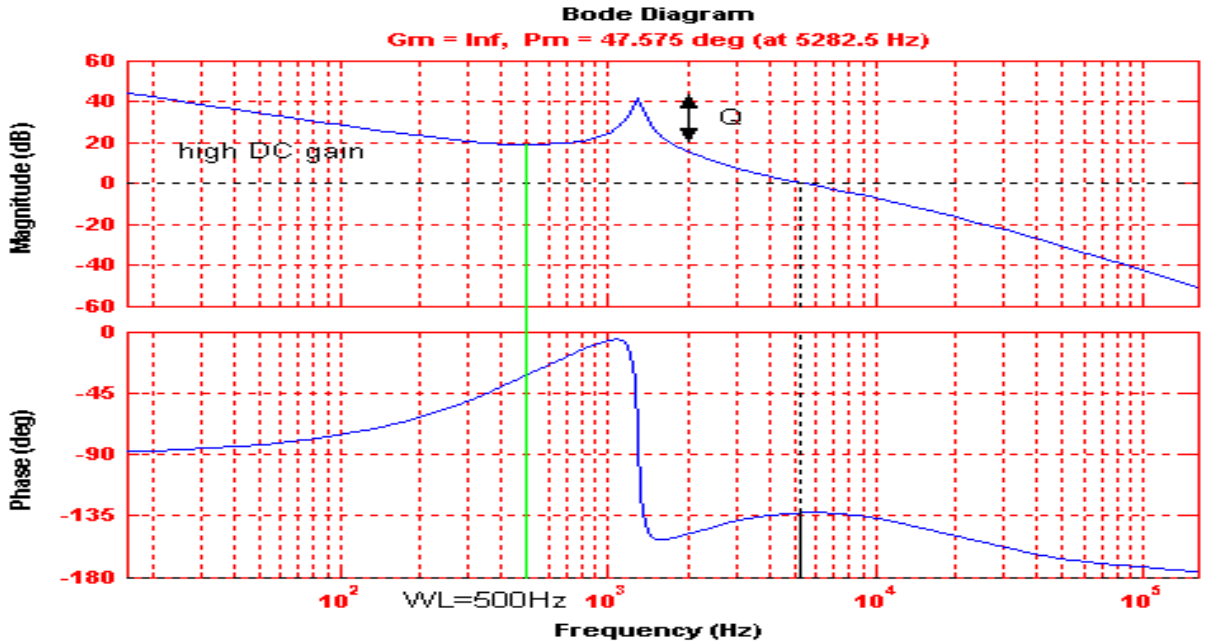


**Figure 4.3: Bode Plot of the open loop system**

## 4.2 Digital PID

Digital PID is commonly used because it is more suitable to design for a complex system for the purpose of reducing cost, and is more immune to noise than an analog PID. Several methods can be used to design a digital PID. One of the methods is to design an analog PID first, then convert the s-domain into the z-domain with appropriate approximation. A digital PID can also be directly designed by the root locus and direct response methods.

### 4.2.1 Conversion from Analog to Digital PID

The conversion from s-domain into z-domain is quick and easy. The conversion can be done by using difference approximation, ZOH (zero-order hold), bilinear transformation or first-order hold. In this section, the difference approximation equation is derived.

The proportional term in PID can be approximated as:

$$K_p e(k) \qquad (4\text{-}7)$$

The backward rectangular rule approximation of integral term in PID:

$$K_I T e(k-1) \tag{4-8}$$

Also, the backward difference approximation of derivative term in PID:

$$\frac{K_D}{T}[e(k)-e(k-1)] \tag{4-9}$$

However, the integral term requires previous information. Thus, the summation of the three terms becomes, where T denotes the sample period.

$$\begin{aligned} u(k) &= K_P e(k) + a(k) + \frac{K_D}{T}[e(k)-e(k-1)] \\ a(k) &= a(k-1) + K_I T e(k-1) \end{aligned} \tag{4-10}$$

Equation 4-10 is the position algorithm of the present control output. The velocity algorithm for the PID is:

$$\begin{aligned} u(k-1) &= K_P e(k-1) + a(k-1) + \frac{K_D}{T}[e(k-1)-e(k-2)] \\ a(k-1) &= a(k-2) + K_I T e(k-2) \end{aligned} \tag{4-11}$$

By subtracting Equation 4-11 from Equation 4-10, the digital PID is approximated as:

$$u(k)-u(k-1) = K_P[e(k)-e(k-1)] + K_I T e(k-1) + \frac{K_D}{T}[e(k)-2e(k-1)+e(k-2)] \tag{4-13}$$

### 4.2.2 Direct Root Locus Design

Root locus design for a digital PID is similar to an analog PID. Basically, the rules for drawing the root locus for both are the same except that stability, frequency and damping ratio are changed.

In terms of stability, it is suggested that the poles be placed in the right-hand plane, and inside the unit circle. The closer the poles are to the origin, the faster the settling time will be.

The procedure to design a digital PID is exactly the same as an analog PID, where the poles and zeros work together to shape the root loci to the desired location.

Even though there is no need to physically build a controller algorithm as the analog PID, one needs to consider whether the digital PID is realizable (*i.e.* the controller does not requires future variables). If the controller is not programmable, the digital PID needs to be redesigned. Modification such as adding another pole inside the unit circle can possibly make the controller realizable.

### 4.2.3 Direct Frequency Design

Direct frequency design is useful especially in deadbeat control, a method to make the system meet commands one sample time later than the desired time.

Using direct frequency design, system requirements are first considered, and written in the form of a transfer function. The controller and system transfer function is set equal to the desired transfer function. Then, the proportional, integral and derivative terms can be solved. This is illustrated in Equation 4-14

$$T(z) = \frac{C(z)}{R(z)} = \frac{D(z)G(z)}{1 + D(z)G(z)} \qquad (4\text{-}14)$$

.

In Equation 4-14, T(z) represents the desired transfer function, C(z) represents sampled system output, R(z) represents sampled system desired input, D(z) represents a controller transfer function, and G(z) represents a discrete system transfer function.

Again, the digital PID must be programmable, so that it does not require the knowledge of future variables.

# CHAPTER 5

# PROPOSED FPID CONTROLLER

# 5. Introduction

This chapter presents a development of a self-tuning fuzzy PID controller to overcome the appearance of nonlinearities and uncertainties in the system. The self-tuning fuzzy PID controller is the combination of a classical PID and fuzzy controller. The controller is designed based on the expert knowledge of the system. Fuzzy logic is used to tune each parameter of PID controller. Appropriate fuzzy rules are designed to tune the parameter $K_P$, $K_I$ and $K_D$ of the PID controller, the performance of the buck converter has improved significantly compare to conventional PID and Fuzzy controllers.

## 5.1 Fuzzy Logic Overview

Fuzzy Logic is a piecewise linear method of data analysis based on using non-precise values over a range to determine the correct correspondence to a particular group. Since fuzzy logic is used within the control scheme, explanation of the methodology and terminology is provided.

The fuzzy logic procedure consists of three parts: input fuzzification, input-to-output mapping, and output defuzzification as seen in Figure 5.1. A precise input, such as voltage, current, etc is measured. The input is the fuzzified by mapping it to a set of input membership functions, through a set of inference procedures. Once the membership to the input functions is determined, the input is mapped to the output membership functions according to a rule base. The rule base is unique to the system and based on expert knowledge. The degree of belonging to the output membership functions is determined and is used to produce a precise output through defuzzification or another inference procedure.

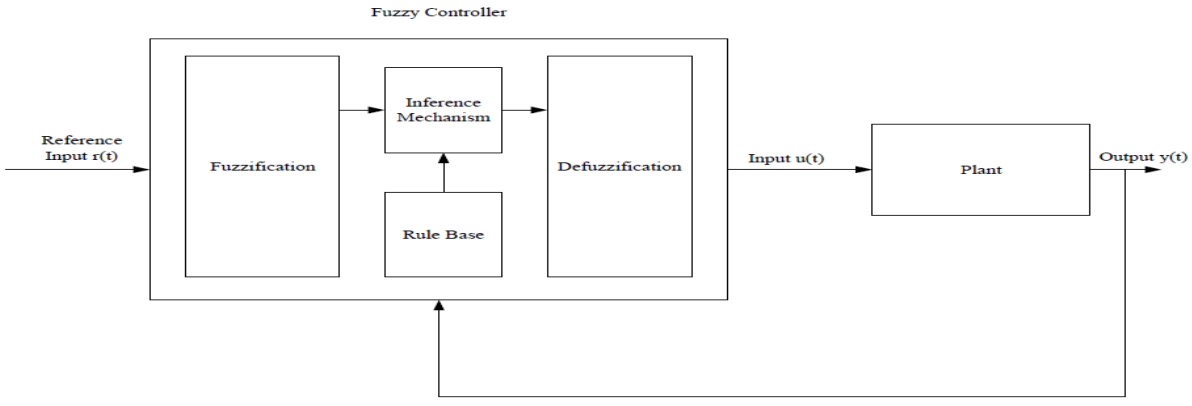


**Figure 5.1: Block diagram of fuzzy control system**

### 5.1.1 Fuzzy Logic Naming Conventions

Fuzzy logic makes use of linguistic variables to determine relationships instead of numerical variable. For example, the variables used within this thesis to express the error voltage are given the names Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero (ZO), Positive Small (PS), Positive Medium (PM), and Positive Big (PB). In order to determine to which category the input belongs, membership functions are needed in order to show the degree of belonging to each particular variable.

### 5.1.2 Membership Functions

Membership functions are graphical mappings to determine how close or how much something belongs to a particular group. Membership functions can be almost any arbitrary shape though some common ones are triangular, trapezoidal, or bell-shaped, as in Figure 5.2. The membership functions are combined over the total domain to produce fuzzy sets. The degree which an input belongs to each membership function in the fuzzy sets is determined through the inference procedure.

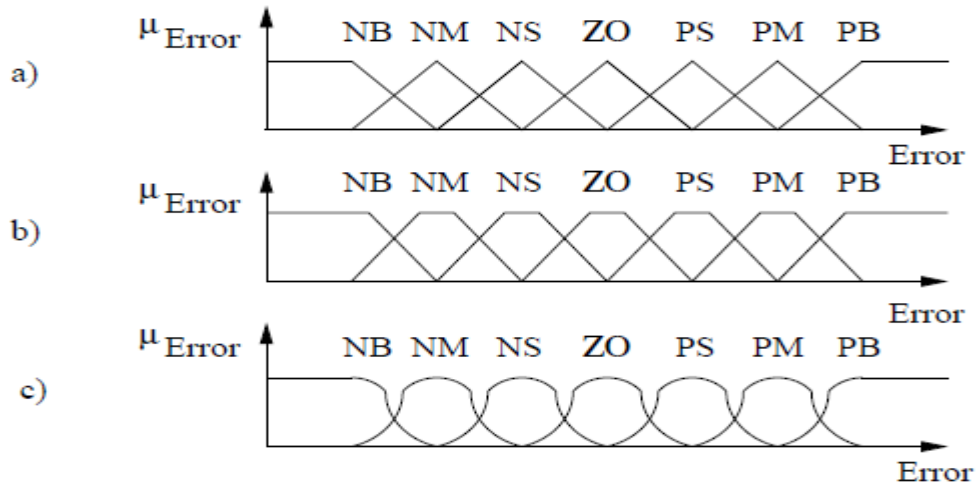


**Figure 5.2: Membership function shapes: a) triangular, b) trapezoidal, and c) bell-shaped.**

### 5.1.3 Fuzzy Operations

In order to understand the inference procedure, the basic fuzzy operation and the rule base are explained. A set of rules for the interaction of the membership functions within the fuzzy sets is defined since membership function overlap. The basic set rules/operations are union, intersection, and complement. Let A and B be the fuzzy sets in U with membership functions $\mu_A$ and $\mu_B$ where U is universe of discourse over the range of all possible input values x.

1. Union

   The membership function $\mu_{(A\cup B)}$ of the union $A \cup B$ is defined for all $x \in U$ by

   $$\mu_{(A\cup B)(x)} = max\ (\mu_A(x), \mu_B(x))$$

2. Intersection

   The membership function $\mu_{(A\cap B)}$ of the intersection of $A \cap B$ is defined for all $x \in U$ by

   $$\mu_{(A\cap B)}(x) = min\ (\mu_A(x), \mu_B(x))$$

3. Complement

   The membership of the function $\mu_{\overline{A}}$ of the complement of fuzzy set $A$ is defined for all $x \in U$

Each of the operations: union, intersection, and complement are graphically displayed in Figure 5.3.

### 5.1.4 Fuzzy Rule/Fuzzy Rule Bases

A fuzzy rule is mapping from the input domain to the output domain. The fuzzy rule is typically based on expert knowledge of the system. Usually fuzzy rules follow an if.. then.. structure, where

If x is A, and y is B, then z is C

Where x and y are the input fuzzy variables; z is the output fuzzy variable; A, B, and C are the fuzzy subsets corresponding to the universe of discourse of X, Y, and Z respectfully. Therefore, if there are n fuzzy rules defined as

R1: If x is A1, and y is B1, then z is C1

R2: If x is A2, and y is B2, then z is C2

R3: If x is A3, and y is B3, then z is C3

.....

.....

Rn: If x is An, and y is Bn, then z is Cn

The rule base, R, is defined as the union of the individual rules. An example rule base is shown in figure 5.4. The rule base may also by presented graphically as a surface similar to Figure 5.5

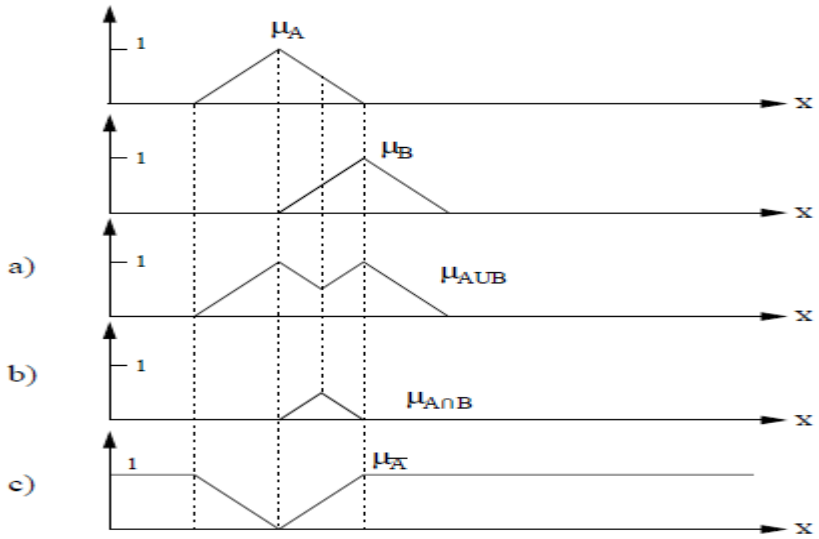


**Figure 5.3: Fuzzy Operations a) union, b) intersection, and c) complement.**

| Δerror \ error | NB | NM | NS | ZO | PS | PM | PB |
|---|---|---|---|---|---|---|---|
| NB | NB | NB | NB | NB | NM | NS | ZO |
| NM | NB | NB | NB | NM | NS | ZO | PS |
| NS | NB | NB | NM | NS | ZO | PS | PM |
| ZO | NB | NM | NS | ZO | PS | PM | PB |
| PS | NM | NS | ZO | PS | PM | PB | PB |
| PM | NS | ZO | PS | PM | PB | PB | PB |
| PB | ZO | PS | PM | PB | PB | PB | PB |

**Figure 5.4: Fuzzy model rule base with two input and single output.**

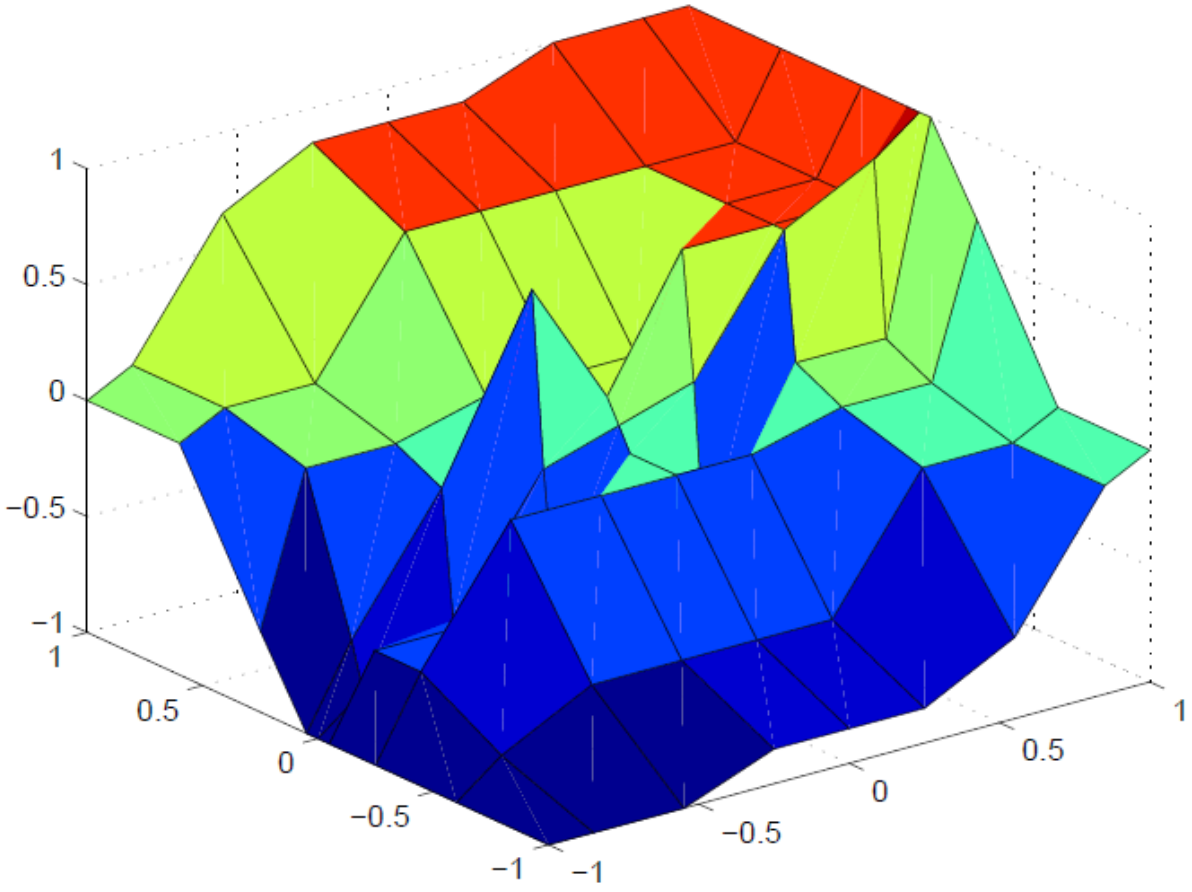


**Figure 5.5: Fuzzy model rule base with two input and single output shown as a surface**

### 5.1.5 Inference Procedure

The inference procedure determines the degree of correlation between the rules and the input. Since the input is typically involves more than one membership function, the inference is used to decide how much of each rule to utilize. Two methods are typically used, inference with min as conjunction or inference with product as conjunction. Assuming the following rule,

R: if x is A then z is C

Where x as the input fuzzy variable; z the output fuzzy variable; and A and C are the fuzzy subsets corresponding of the universe of discourse of X and Z respectfully. The degree of correlation would correspond to the membership of x to A

$$r = \mu_A(x)$$

$$c' = min(c, r)$$

or

$$\mu'_c(r) = min(\mu_c(r), r)$$

for all z $\in$ Z.

Similary, the degree of correlation for the production of conjunction

$$r = \mu_A(u)$$

$$c' = c * r$$

or

$$\mu'_c(z) = \mu_c(z) * r$$

for all z $\in$ Z.

### 5.1.6 Defuzzification

The center of average method is used to obtain the fuzzy controller's output δd[k], which is given by Equation 5-1. When using triangle-shaped membership functions, there are at most four rules that are effective at any one time; therefore, n=4.

$$\frac{\sum_{j=1}^{n} \mu_{A_j}(u) C_{ji}}{\sum_{j=1}^{n} \mu_{A_j}(u)} \qquad (5\text{-}1)$$

## 5.2 OVERVIEW OF FUZZY PID CONTROLLER

Fuzzy PID controllers in literature can be classified into three major categories as direct action type, fuzzy gain scheduling type, and hybrid type fuzzy PID controllers [5]. The direct action type can also be classified into three categories according to number of inputs as single input, double input, and triple input direct action fuzzy PID controllers. The classification of fuzzy PID controllers can be seen in Figure 5.6.

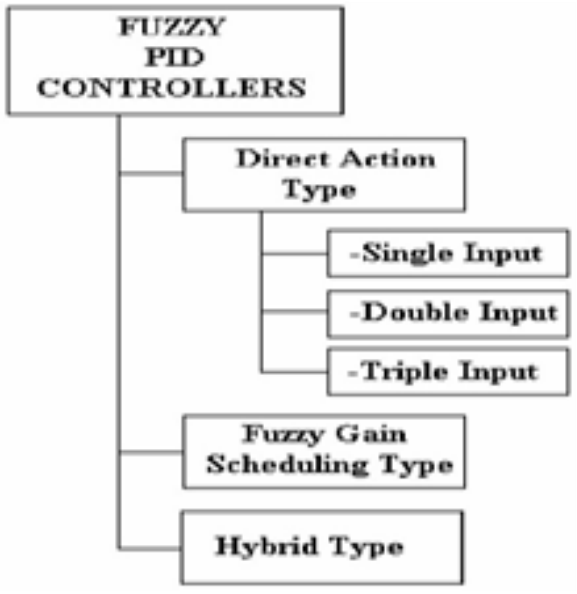


**Figure 5.6: classification of fuzzy PID controller**

### 5.2.1. SINGLE INPUT FUZZY PID CONTROLLER

This structure uses error as the only input and has a one dimensional rule-base. As it is seen in Figure 5.7, it is simply a nonlinear mapping of error into fuzzy proportional action cascaded to a conventional PID controller.

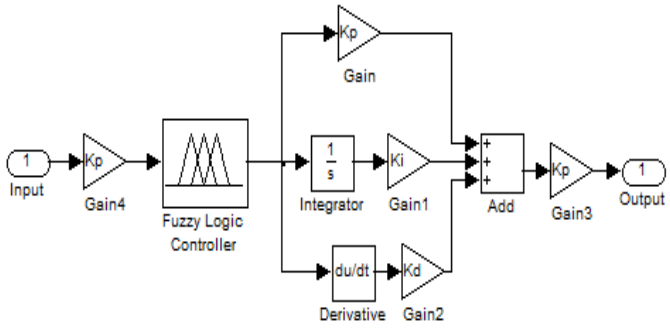


**Figure 5.7: single input fuzzy PID controller**

## 5.3 PROPOSED SELF-TUNING FUZZY PID CONTROLLER

The proposed controller that is given in Figure 5.8 is the modified version of the single input fuzzy PID controller. It possesses two main parts: the classical PID and fuzzy controllers. A standard PID controller is also known as the "three-term" controller, whose transfer function is generally written in the "ideal form" as

$$G_{PID}(s) = K_P + \frac{K_I}{S} + K_D S \qquad (5-2)$$

Where $K_P$ is the proportional gain, $K_I$ is the integral gain and $K_D$ is the derivative gain. The ''three-term'' functionality is highlighted by the following:

- The proportional term is providing an overall control action proportional to the error signal through the all-pass gain factor.
- The integral term is reducing steady-state errors through low-frequency compensation by an integrator.
- The derivative term is improving transient response through high-frequency compensation.

In this thesis the fuzzy controller will be used to tune the parameter $K_P$, $K_I$ and $K_D$ of the PID controller, based on certain function of the actuating error signal.

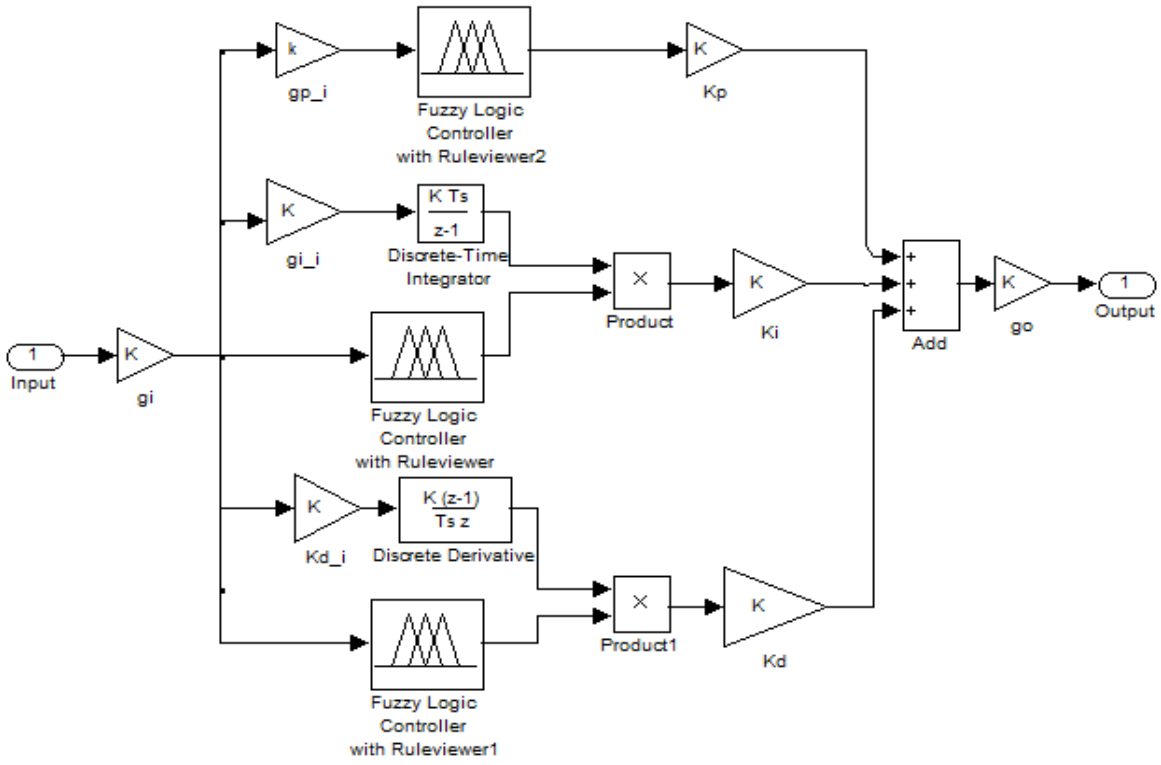


**Figure 5.8: Simulink model of self-tuning FPID controller**

## 5.4 CONTROLLER DEVELOPMENT

In this section a self-tuning fuzzy PID controller is developed. The FPID controller consists of three parallel fuzzy sub controllers, namely, fuzzy-based proportional, integral, and derivative controllers. These independent controllers are grouped together to form an intelligent self-tuning fuzzy PID controller. The FPID controller can account for nonlinearity and adaptable to varying operating condition.

### 5.4.1 Input scaling

Since the inference procedure is designed to only operate within the bounds [-1, 1] the input into the fuzzy logic controller is bounded within the universe of discourse between [-1, 1]. The input to the fuzzy controller is directly connected to the output of the ADC. Therefore the input gain $g_i$, should be selected such that $V_{OADC} g_i \in [-1, 1]$.

### 5.4.2 Control Gain Coefficient

At the first stage of designing process, discrete model of the conventional PID controller is obtained. Then FPID controller, as shown in Figure 6.4, is obtained which has six tuning control parameters: $g_{ip,}$ $g_{ii}$, $g_{id}$, $K_P$, $K_I$, and $K_D$. In order to simplify the calculations $g_{ip,}$=1 and $g_{ii}$= $g_{id}$,=T can be considered [6]. A Ziegler-Nichols method is used to determine the initial values of $K_P$, $K_I$, $K_D$ for a specific set point.

Since the performance of FPID controller depends on the gains coefficients, it is obvious that the optimization of these parameters will lead to better performance at a particular set point [7].

### 5.4.3 Fuzzy-Based Proportional Controller

The first step in designing the controller is to decide which state variables of the system can be taken as the input signal to the controller. The output voltage error e[k] is used as the input to the controller. The output of the fuzzy-based proportional controller is the gain $K_P$. The universe of discourse of interval spanned by the input variable is partitioned into seven fuzzy subsets of Gaussian shaped membership functions assigning each subset a linguistic value; the various subset are presented as NB (Negative Big), NM (Negative Medium ), NS (Negative Small), Z (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big) respectively. The main advantage to employ Gaussian function is that its continuity is usually required for most of conventional gradient-based, either first or second order optimization technique [9].

The second step in the design of the fuzzy sub controller is the determination of the fuzzy IF-THEN inference rules. The number of fuzzy rules that are required is equal to the number of fuzzy sets of the input variable. Thus, a total of seven fuzzy rules are required to relate each possible combination of the input variable to the output membership fuzzy sets. A typical rule can be written as follow. IF e[k] is NB THEN $K_P$ is NB.

The derivation of the fuzzy control rules is heuristic in nature and based on the following criteria [10]:

- When the output of the converter is far from set point, the change of $K_P$ must be large so as to bring the output to the set point quickly.
- When the output of the converter is approaching the set point, a small change of $K_P$ is necessary.

- When the output of the converter is near the set point and is approaching it rapidly, the $K_P$ must be kept constant so as to prevent overshoot.
- When the set point is reached and the output is still changing, the $K_P$ must be changed a little bit to prevent the output from moving away.
- When the set point is reached and the output is steady, the $K_P$ remains unchanged.
- When the output is above the set point, the sign of the change of $K_P$ must be negative, and vice versa.

The next step in the design of the fuzzy sub controller is inference mechanism. The results of the inference mechanism include the weight factor $W_i$ and the change in $K_P$ $c_i$ of the individual rule. The weight factor $W_i$ is obtained by Mamdani's min fuzzy implication of $\mu_e$ (e[k]), $\mu_{ce}$ is the membership degrees [9]. Control $c_i$ is taken from the rule base. The change in $K_P$ inferred by the $z_i = w_i * c_i$ is given by

$$\min\{\mu_e(e[k]) * c_i\} \qquad (5-3)$$

The last step in the design of the fuzzy sub controller is the defuzzification process. The input for the defuzzification process is a fuzzy set (the aggregate output fuzzy set) and the output obtained is also aggregated fuzzy output. But generally, it is required that the output be a single crisp number. As the aggregated fuzzy set encompasses a range of output values, it must be defuzzified in order to resolve to a single crisp output value from the set. The center of average method is used to obtain the fuzzy controller's output for the control of buck converter.

The proportional gain control surface needs to minimize the rise time, the overshoot and steady-state error. In order to improve the rise time, overshoot, and steady-state error, the centers for the input and output fuzzy sets are chosen, shown in figure 5.9. The control surface corresponding to these centers can be seen in figure 5.10.

| | NB2 | NB2 | NB | NM | NS | ZO | PS | PM | PB | PB2 | PB3 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Input | -1 | -0.9 | -0.8 | -0.12 | -0.01 | 0 | 0.01 | 0.12 | 0.8 | 0.9 | 1 |
| Output | 1 | -0.6 | -0.42 | -0.3 | -0.1 | 0 | 0.1 | 0.3 | 0.42 | 0.6 | 1 |

**Figure 5.9: Centers for input/output fuzzy set for proportional gain**

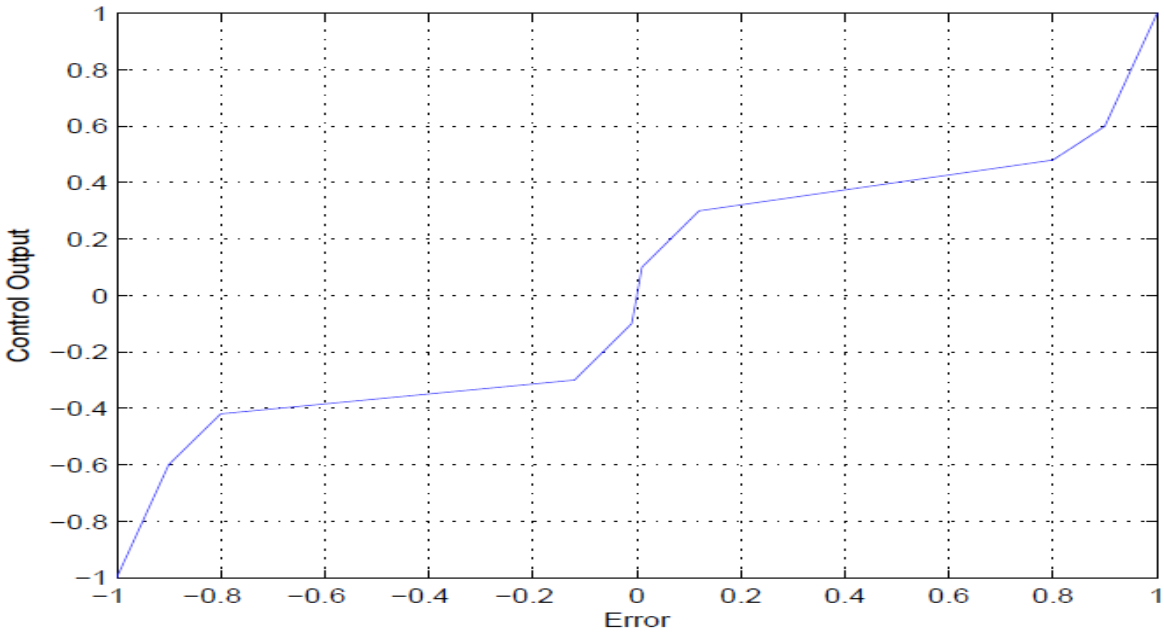


**Figure 5.10: Proportional Gain Control Surface**

### 5.4.4 Fuzzy-Based Integral Controller

The same technique applied to the fuzzy-based proportional controller is applied to the fuzzy-based integral controller. The controller has single input the output voltage error e[k]. The output of the fuzzy-based integral controller is the gain $K_I$. Seven fuzzy sets are defined for the fuzzy linguistic variable e[k]. After specifying the fuzzy sets of the fuzzy variable, the membership function for these sets are derived. The membership functions are composed of the same fuzzy Gaussian membership functions allocated for the fuzzy based proportional controller. Similarly, the number of fuzzy rules that are required is equal to the number of fuzzy sets that the input variable makes. Therefore, a total of seven fuzzy rules are introduced. The same Mamdani's

min fuzzy implication of $\mu_e(e[k])$ is used for the inference mechanism. For the defuzzification process the center of average method is used to obtain the fuzzy controller's output for the control of buck converter

The integral control surface needs reduce the steady-state error to zero while still maintaining the overall stability of the system. In order to reduce the steady-state error while still maintaining stability, the centers for the input and output fuzzy sets are chosen, shown in figure 5.11. The control surface corresponding to these centers can be seen in figure 5.12.

| | NB2 | NB2 | NB | NM | NS | ZO | PS | PM | PB | PB2 | PB3 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Input | -1 | -0.35 | -0.1 | -0.01 | -0.005 | 0 | 0.005 | 0.01 | 0.1 | 0.35 | 1 |
| Output | 1 | -1 | -0.4 | -0.2 | -0.01 | 0 | 0.01 | 0.2 | 0.4 | 1 | 1 |

**Figure 5.11: Centers for input/output fuzzy set for integral gain.**

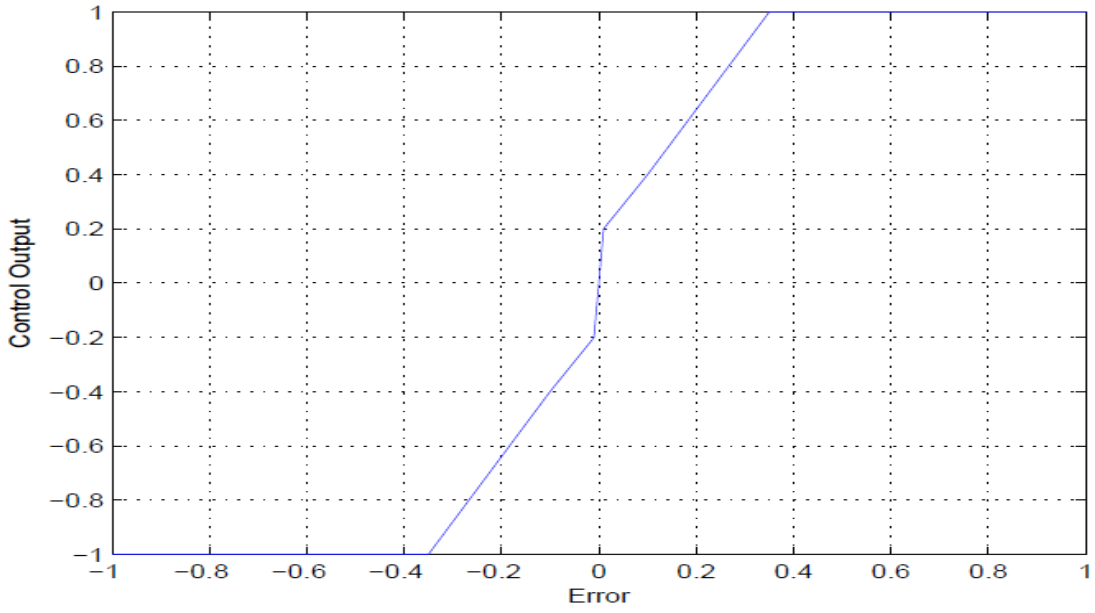


**Figure 5.12: Integral Gain Control Surface**

### 5.4.5 Fuzzy-Based Derivative Controller

The same process applied to fuzzy-based proportional and integral controller is applied to the fuzzy-based derivative controller. The input signal to the controller is the error signal e[k]. The output of the controller is the gain $K_{D.}$ Seven fuzzy sets are defined for the fuzzy linguistic variable e[k]. The same fuzzy Gaussian membership functions allocated for the fuzzy based proportional and integral controller are used for these fuzzy sets

The derivative control surface needs to increase the stability and decrease the over-shoot of system, while having little impact on the speed of the system. In order to decrease the overshoot and increase the stability of the system, the centers for the input and output fuzzy sets are chosen, shown in figure 5.13. The control surface corresponding to these centers can be seen in figure 5.14.

| | NB | NM | NS | ZO | PS | PM | PB |
|---|---|---|---|---|---|---|---|
| Input | -1 | -0.2 | -0.02 | 0 | 0.02 | 0.2 | 1 |
| Output | -1 | -0.8 | -0.2 | 0 | 0.2 | 0.8 | 1 |

**Figure 5.13: Centres for input/output fuzzy set for derivative gain**

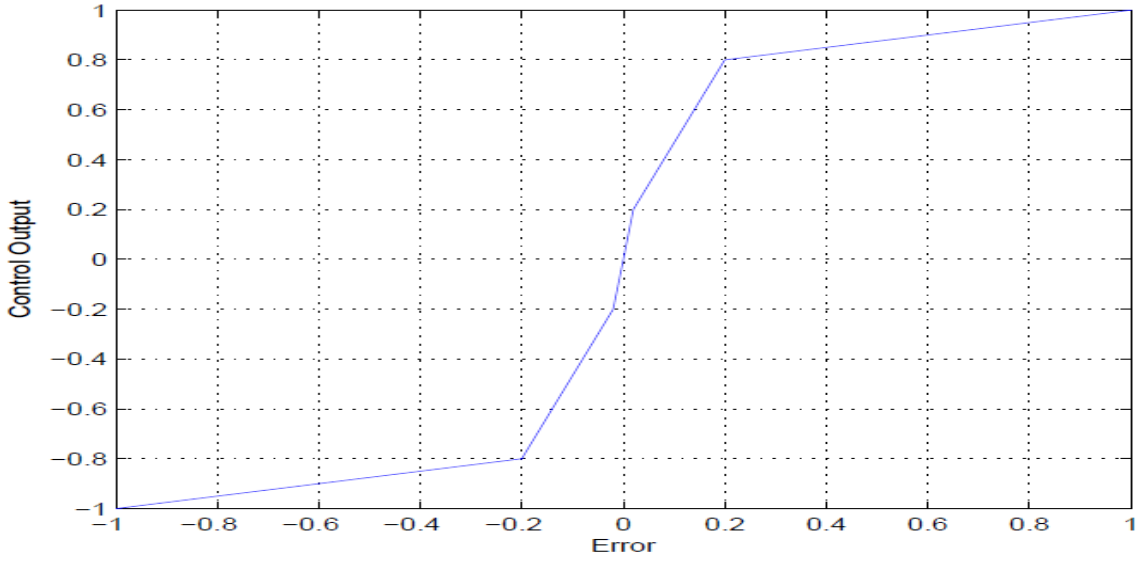


**Figure 5.14: Derivative Gain Control Surface**

### 5.4.6 Output Scaling

Output scaling allows the output of the FPID controller to be adjusted so it has the appropriate amplitude when applied to the DPWM of the buck converter. The FPID controller output is bounded in the universe of discourse between [-1, 1]. The change in duty cycle control ratio of the DPWM is bounded between [-D, 1-D], therefore the output gain must be selected such that $V_{oFPID}g_o \in$ [-D, 1-D], since $V_{oFPID}$=a, it is already bounded between [-D, 1-D] and $g_0$=1.

# CHAPTER 6

# DSP IMPLEMETATION FOR DIGITAL CONTROLLERS

# 6. Introduction

Power electronics systems are typically a complex combination of linear, nonlinear and switching elements. High-frequency converters add another dimension of complexity because of their fast dynamics. Real-time power electronics systems, therefore, demand the use of high-speed data acquisition and control. DSPs (Digital Signal Processors) meet the processing requirements posed by such systems. DSPs are used in multiple applications in power electronics including AC motor drives, high-frequency converter control, motion control, robotics and real-time testing and monitoring.

## 6.1 Overview of DSPs

Because of the DSP's special architecture, it is more useful than a general-purpose microprocessor for the high-speed processing applications and real-time systems such as control system. DSPs are built with Harvard architecture, and this configuration employs separate program and data buses [14]-[17]. The benefit of this arrangement is the increased speed because instructions and data can move in parallel instead of sequentially. DSPs, like many advanced microprocessors, use pipelining to operate on several instructions simultaneously.

- Hard-Wired Logic: In DSPs, most instructions execute in one machine cycle because all functions are performed internally in hard-wired logic. Hardware multipliers in DSPs perform multiplication in a single cycle.
- Scaling: Hardware shifters allow the scaling of data used in computations. This helps prevent overflows and keep the required precision.
- Saturation: In DSPs, the accumulator handles overflow by saturating to the most positive or least negative value, thus eliminating rolling over.
- Word Length: Some DSPs support a large word length, thus reducing the quantization error. They also support a larger intermediate word length for intermediate computational results.
- Other Features: Many DSP chips include input/output (I/O) functionality, timing circuitry, direct memory access (DMA) controllers and high-speed memories on-chip.

DSPs resemble reduced instruction set computers (RISCs), in that a small set of frequently used instructions are optimized for numerical processing at the expense of less

frequently used general-purpose operations. DSP instruction sets efficiently handle mathematical operations common to many algorithms that are repeatedly executed in time-critical loops. For example, digital filters which are often used in signal processing and control applications, are implemented using recursive difference equations of the form:

$$y(n) = \sum_{i=0}^{N} a(i)x(n-i) + \sum_{j=1}^{M} b(j)y(n-j)$$

The equation states that any output can be computed as a weighted sum of the input at the present time, past inputs and past outputs. Each step in this computation involves a multiplication and addition. The multiply and accumulate (MAC) instruction in DSPs performs this in a single instruction cycle. In contrast, in a typical fixed-point microprocessor, a "multiply" and "add" typically executes in 15 to 20 machine cycles. MAC is the one instruction that most distinguishes DSPs from other micros.

DSPs also significantly increase execution speed by performing multiple operations in parallel. For instance, in the same instruction cycle that a MAC operation is being performed, a parallel data move can be carried out. Thus, the special DSP instructions supplement the computational speed of DSPs and make them ideal for high-performance real-time applications.

## 6.3 Architecture of TI C2000 and TMS320F2812

TI has developed the DSP solutions that are driving digital control by providing the industry's high performing and code efficient DSPs. The TMS320C2000 family of DSP controllers set the standard for performance and peripheral integration by offering a unique combination of on-chip peripherals such as flash memory, ultra-fast A/D converters, PWM modules and robust CAN modules.

TMS320C2812 is a member of the TMS320C28x DSP generation, which is a highly integrated, high-performance solution for demanding control applications [16]-[17]. These devices are based on a 32-bits DSP core delivering 150 MIPS of performance on a flash process and an impressive 32x32bit MAC in a single 6.67ns cycle. These DSPs also uniquely feature a large amount of fast-access on-chip flash memory so that code can be executed internally without adding costly external flash memories. Furthermore, these devices incorporate a high-

precision ultra-fast ADC together with many control and communication peripherals for truly single-chip designs. Figure 6.1 is the architecture of the TMS320C2812.

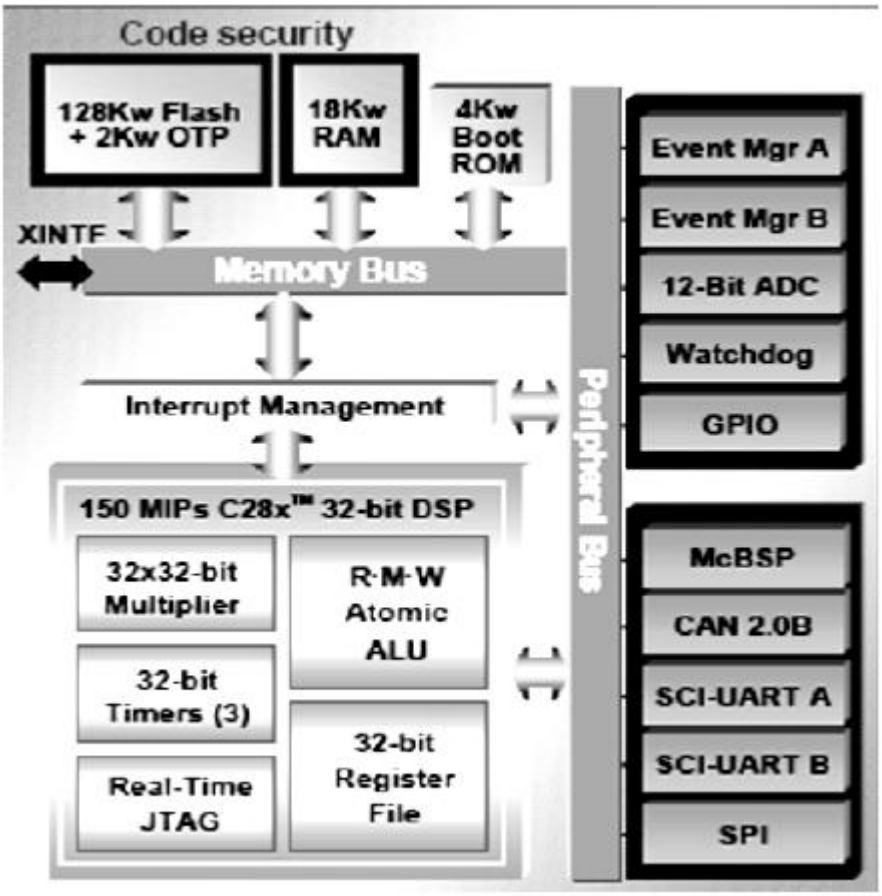


**Figure 6.1: Architecture of TMS320C2812**

Due to its architecture, which is specially optimized for C/C++, these devices offer good code efficiency, and give customers the ability to develop their algorithms entirely in high-level languages. Further, these devices uniquely enable customers to develop their code in virtual floating point via the IQ math capability.

The TMS320C2812 supports multiple bus architecture, whose memory bus architecture contains a program read bus, and data read bus and data write bus. The 32-bit-wide data busses enable single cycle 32-bit operations. The F281x and C281x implement the standard IEEE 1149.1 JTAG interface. Additionally, the TMS320C2812 supports the real-time JTAG mode of operation including the contents of memory, peripheral and register locations; that is to say, the

real time analysis is allowed. It contains 128K x 16 of embedded Flash memory and 128K x 16 of ROM, and two blocks of single access memory, each 1K x 16 in size. The TMS320C2812 supports the 32-bits CPU timers and several serial communication peripherals including CAN, McBSP, SPI and SCI. Further, it supports the event managers and ADC as peripherals, which are used for embedded control and communication.

### 6.3.1 PWM Generators and ADC of TMS320F2812

With digital power applications, ADC and PWM modules are the most important peripheral devices inside the DSPs. TMS320F2812 provides high performance ADC and PWM generators and makes it possible to meet the high requirement of DC-DC converters.

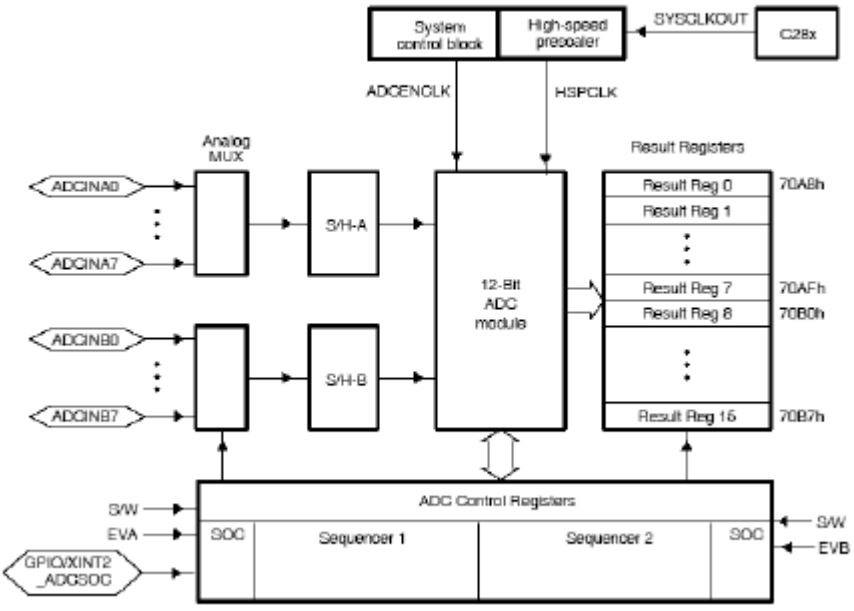


**Figure 6.2: Structure of ADC in TMS320F2812**

The ADC of TMS320F2812 provides 12-bit core with built-in dual sample-and-hold (S/H), simultaneous sampling or sequential sampling modes, very fast conversion time (running at 25 MHz), ADC clock, or 12.5 MSPS, and 16-channel, multiplexed inputs and 16 result registers to store conversion values. The sequencer of ADC can be operated as two independent 8-state sequencers or as one large 16-state sequencer. The ADC interrupts can be triggered by multiple

sources for the start-of-conversion (SOC) sequence, such as S/W — software immediate start, event manager A/B or the external pins.

The PWM modules of TMS320F2812 are designed to generate pulse width modulated waveforms used in motor control and motion control applications. The PWM waveform generation capability of each event manager module (A and B) is summarized as follows.

There are five independent PWM outputs — three of which are generated by the compare units, while the other two are generated by the GP timer compares — plus three additional PWM outputs, dependent on the three compare unit PWM outputs. TMS320F2812 provides programmable dead-band for the PWM output pairs, and the minimum dead-band duration of one device clock cycle (6.67ns). The minimum PWM pulse width and pulse width increment/decrement is one clock cycle. The PWM supports 16-bit maximum PWM resolution and programmable generation of asymmetric, symmetric and space vector PWM waveforms. Figure 6.3 is an example of generating the PWM waveform with the controlled dead time based on the given PWM period and initial values.

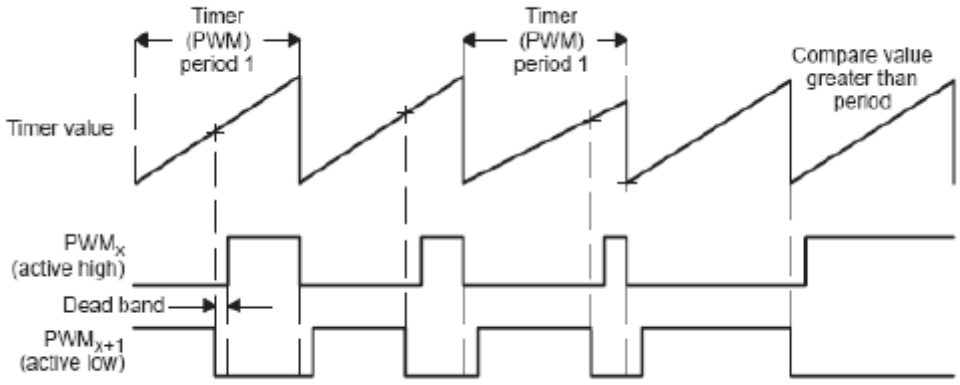


**Figure 6.3: Generating the PWM waveform in TMS320F2812**

## 6.4 Controller Implementation with TMS320F2812

### 6.4.1 ADC Implementation

The ADC of TMS320F2812 could be triggered by the software, EVA/B or the external pins. In our DSP platform, we set up the ADC triggered by the Event Timer A, whose frequency is

supposed to be equal to the sampling frequency of ADC, since the SOC of ADC is designed to be triggered by the underflow of the timer ramp signal, as shown in Figure 6.4.

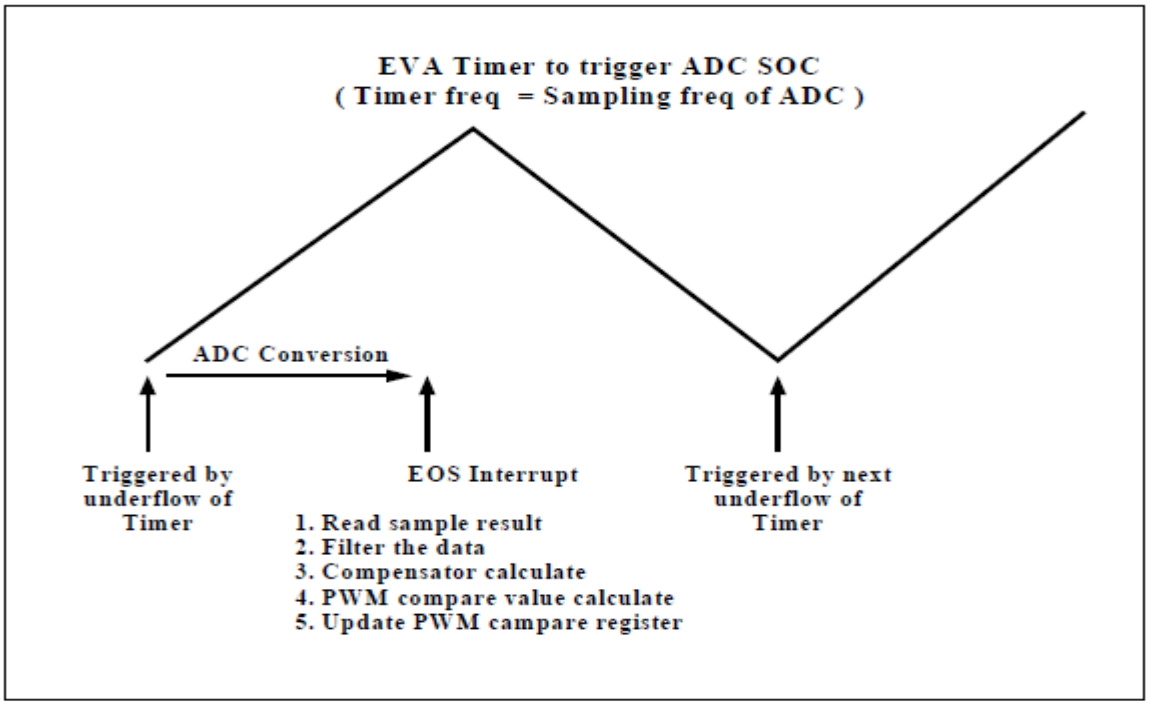


**Figure 6.4: Set-up of ADC**

The SOC (start of conversion) is started by the Timer A, and once the conversion is finished, the EOC (end of conversion) interrupt is triggered, and then the ADC interrupt routine is called in the program. In ADC interrupt routine, DSP first reads the sample result from the ADC result registers and then processes the data, such as filtering or averaging the data. After that, DSP calculates the compensator and gets the result, which is supposed to be the new value of the duty cycle. Finally, the PWM modulated value is calculated in terms of the new duty cycle, and then the registers are updated before the next trigger of the ADC conversion

### 6.4.2 PWM Implementation

The PWM modules of TMS320F2812 can set up the period register TxPR and configure register TxCON to initialize the frequency and configuration of PWM. To generate the gate driver signals for the DC-DC converter, the PWM frequency is designed to be equal to the switching

frequency, which is 400 kHz. To avoid the limit cycle, the resolution PWM must be greater than the resolution of ADC. The PWM signal of TMS320F2812 has 16-bits resolution, while the resolution ADC is 12 bits. Therefore, TMS320F2812 provides the most reasonable resolution for the digital controller implementation.

The power stage we are using for the digital control investigation is DC-DC Buck converter. There are two kinds of cases for the converter, which includes symmetrical and asymmetrical cases. For the symmetrical case, the gate signals of primary side have the same duty cycle ratio but with 180-degree phase shift, while for the asymmetrical case, the gate signals of the primary side are complimentary signals with dead time. Further, we should generate the complementary signals with controlled dead time for the secondary side signals. TMS320F2812 can provide the minimum increment of PWM signal or the minimum dead time as one clock cycle 6.67ns, which is supposed to be sufficient for the HB converters requirement.

The figure 6.5 and 6.6 show how to generate the primary and secondary PWM signals with PWM generator of TMS320F2812. To get the accurate dead time and phase shift of the signals, we generate the signals based on the same timer, which is set up in Event Manager A. The symmetrical ramp signals are achieved by using Event Manager A timer in a PWM module. Using given duty cycle values from the compensator calculation, the four compare values are calculated to get responding values, and then the compare registers are set up respectively.

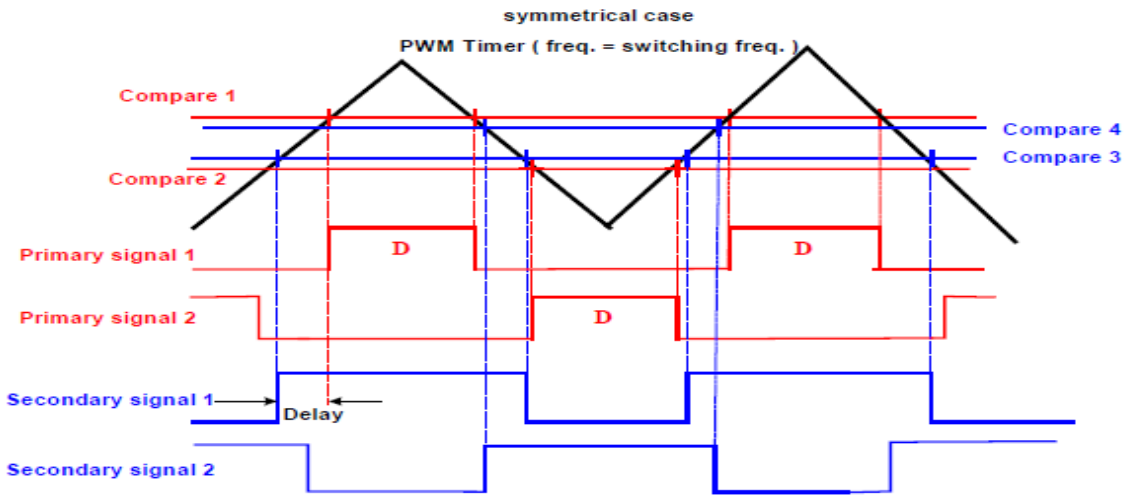


**Figure 6.5: Symmetrical PWM signals generating**

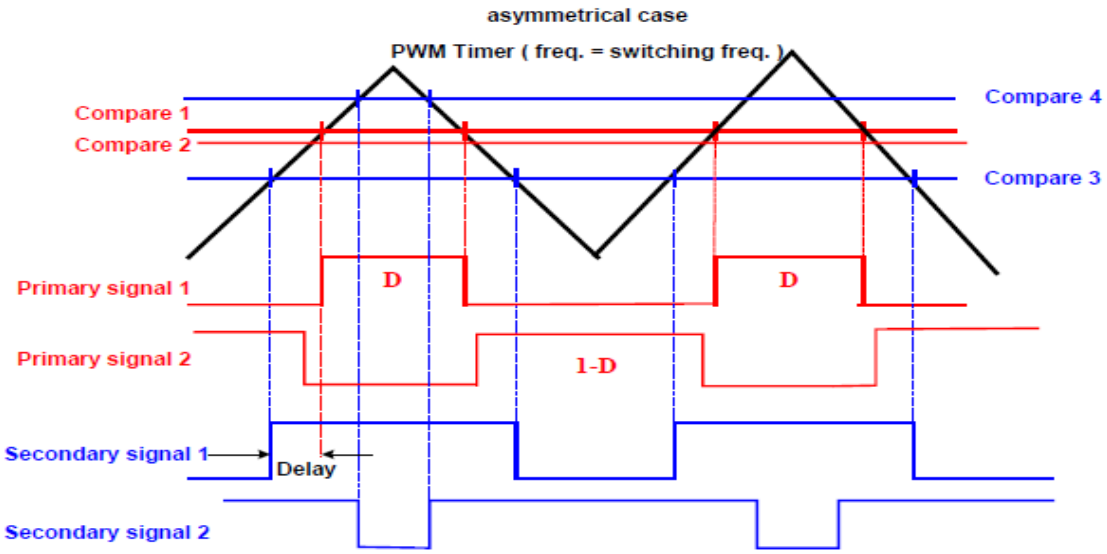


**Figure 6.6: Asymmetrical PWM signals generating**

### 6.4.3 Program Structure

The complete real-time controller implementation is interrupt driven. The PWM module loads the new value of the duty cycle at the beginning of every switching cycle. All calculations regarding the duty cycle are implemented in the ADC interrupt routine. Given the ADC sampling frequency of 1.4MHz, the interrupts are 700ns. Taking into account the interrupt response time, the time available for the processor to compute the new value of the duty cycle is about 700ns or 100 instructions. A flow chart of the controller implementation is shown in Figure 6.9.

In the practical implementation of a controller in DSP, the following critical issues have to be considered:

- The input signals are sampled, and then the signal is filtered by a low-pass filter to reduce the noise. Since the bandwidth of the low-pass filter is going to affect the whole bandwidth of the loop, that bandwidth should be considered carefully.
- The soft start is used to avoid the transient overshoot when a system is started up. In the soft start module, the duty cycle is increased with a small step to avoid a sharp ascend of the output signal.
- The duty cycle is limited from 0 to 0.45 as a protection objective

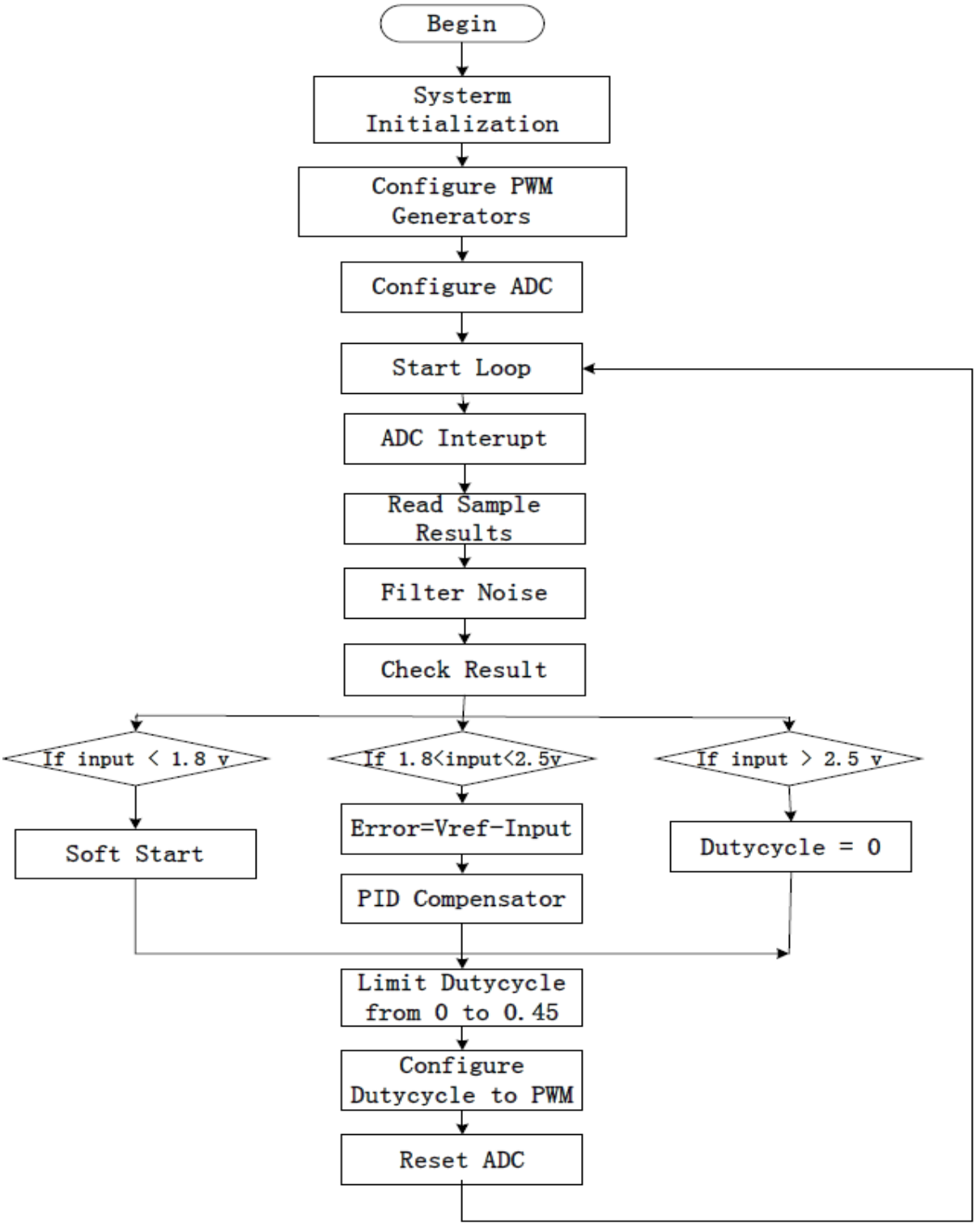


**Figure 6.9: Flow chart of controller implementation in DSP**

# CHAPTER 7

# SIMULATION RESULTS

## 7. Simulated Model of Buck Converter

The MATLAB/Simulink simulation tests the transient and state-state response of the system to various disturbances from the source and load with using the model in Figure 7.1, with the controller regulating the change in the duty cycle. The simulation is designed to compare the open-loop response of the system with the compensated closed-loop response of the system. The conditions simulated are the same as in section 3.9 and consist of the following:

- Connection to the 12 V DC power source
- 1 Amp step change in the load
- 1 volt step change in the power source

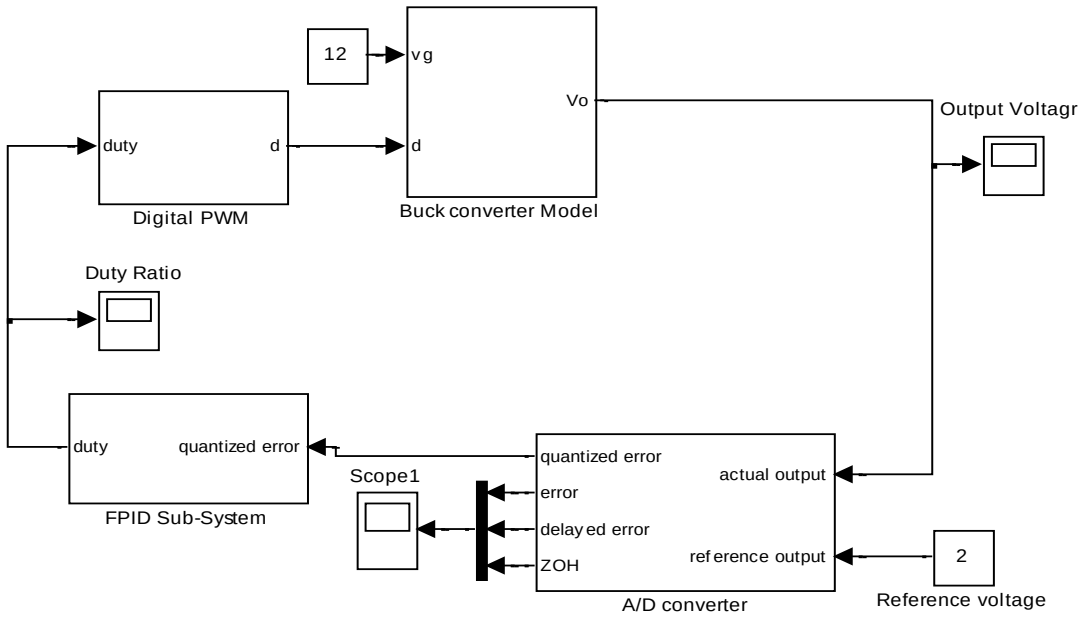


**Figure 7.1: Simulink Model of FPID Compensated Buck Converter**

The controller is a fuzzy logic PID with the control surfaces outline in section 5.4. The controller contains the required input and output gains mentioned in sections 5.4.1 and 5.4.6. The ADC of the controller has a resolution of 4:8828 $10^{-4}$ V and a gain of 0.1, while the DPWM has a resolution of 2:4414 $10^{-4}$ V. Other assumptions made are

- The output ripple due to switching is ignored.
- All other disturbances from the power source, including noise, are ignored.

## 7.1 Simulation Results

Simulation results of buck converter are presented in this section. The Matlab Simulink is used to test the transient and steady-state response of the system to various disturbances from the source and load side. The simulation results are used to compare the open-loop response of the system with the compensated closed-loop response of the system.

### 7.1.1 Response to 12 V DC Power Source

The response of the open-loop system and the system compensated by a fuzzy logic PID controller for a 12 V DC power source can be seen in Figure 7.2. Both responses have zero steady-state error since the initial condition of the duty-cycle, D is 0.2891, is chosen so that is met. The open-loop response has a maximum overshoot of 70 percent while the closed-loop response has a maximum overshoot of 6.5 percent. In addition, the settling time has been reduced from 2.75 msec to 1.10 msec. However, the rise time has been increased from 0.2 msec to 0.6 msec.

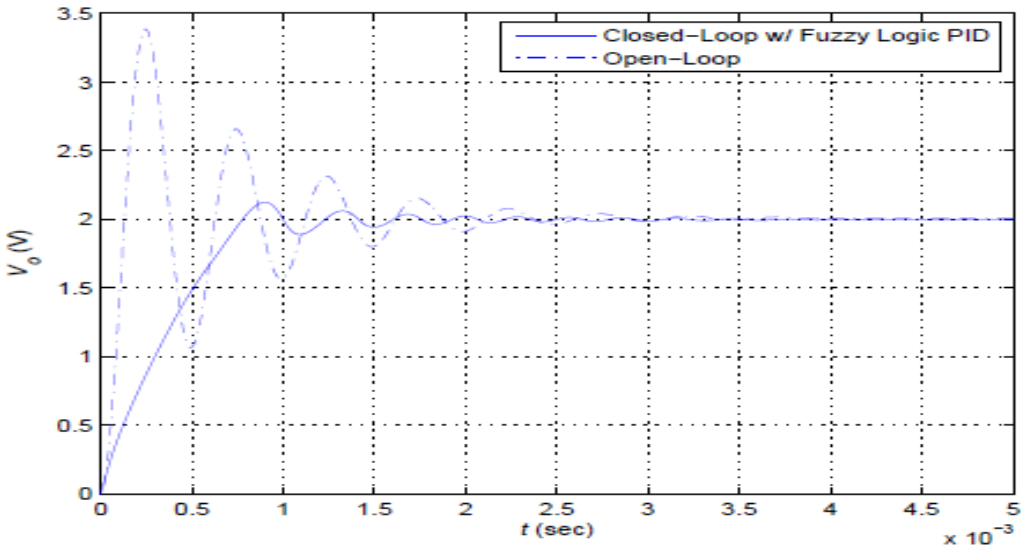


**Figure 7.2: Time response of open-loop and closed-loop system to 12 V DC power source**

### 7.1.2 Response to 1 V Step Change in Power Source

The time response of the open-loop and closed-loop system compensated by a fuzzy logic PID controller for a 1 V step change in the source can be seen in Figure 7.3. The figure shows that

the steady-state error improves from 8 percent to less than 1 percent for the simulation. The steady-state error of the compensated system eventually decreases to zero because of the integral action. In addition, the maximum overshoot improves from 6 percent to less than 1 percent.

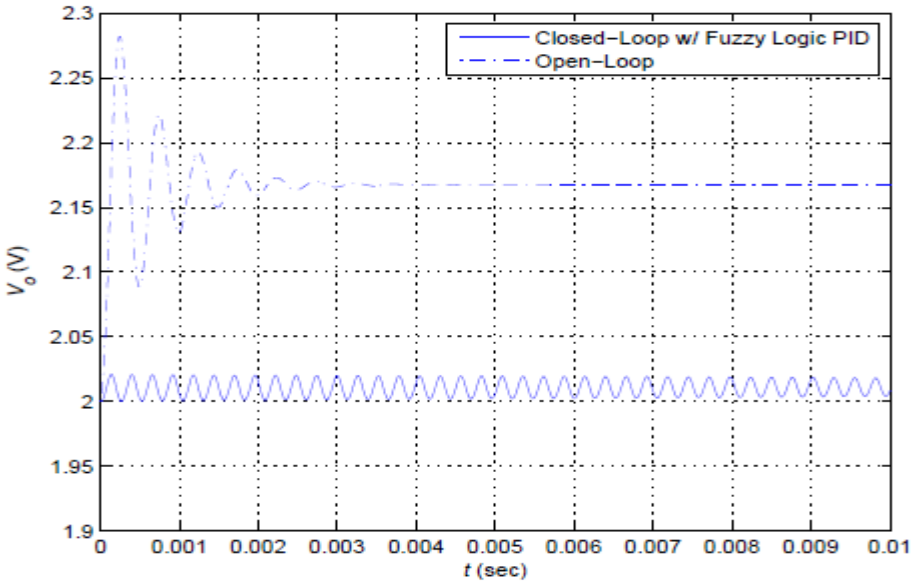


**Figure 7.3: Time response of open-loop and closed-loop system to 1 v step change in power source**

### 7.1.3 Response to 1 A Step Change in Load Current

The time response of the open-loop and closed-loop system compensated by a fuzzy logic PID controller to 1 A step change in the load can be seen in Fig 7.4. It can be seen from this figure that the steady-state error decreases from 1 percent to zero. In addition, the maximum undershoot improves from 12 percent to 3 percent and the maximum overshoot improves from 7 percent to 2 percent.

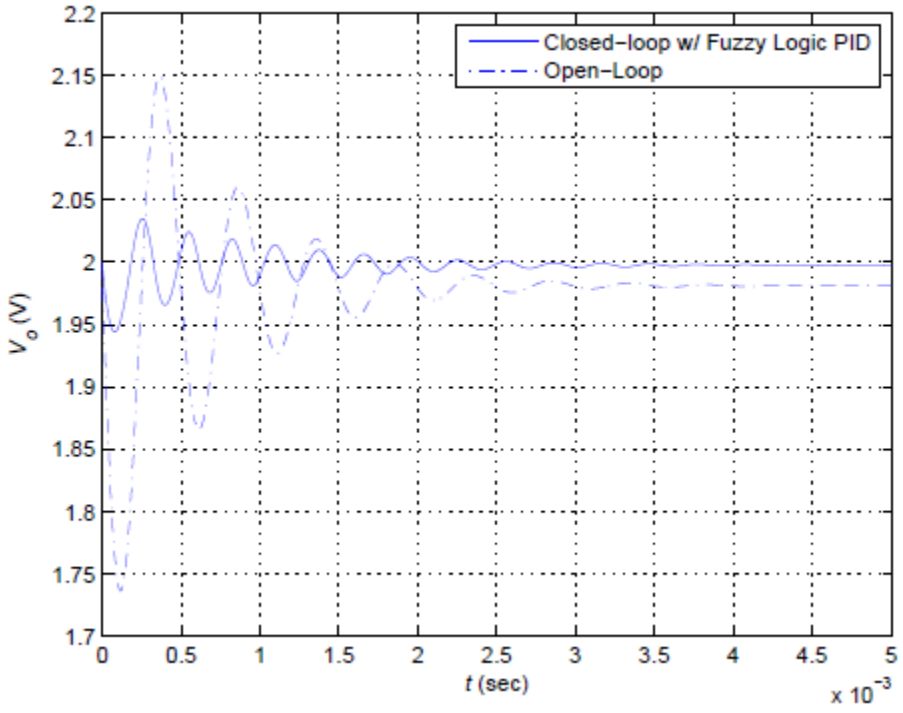


**Figure 7.4: Time response of open-loop and closed-loop system to 1 A step change in load current.**

## 8. Conclusions

Current trends in electronics require operation at low voltages with higher currents. In order to supply power to these electronics, PWM power converters are required which are able to deliver these voltages and currents efficiently. One such converter capable of delivering these requirements is the buck converter. The circuit is capable of generating lower voltages with a more median duty cycle.

In addition, digital control schemes are replacing the use of analog control schemes when controlling PWM power converters. Digital schemes, implemented through the use of DSPs, offer immunity to component variations, digital system compatibility, and the ability to incorporate advanced control schemes which is not available in analog counterparts.

One advanced control scheme which can be implemented with DSP is fuzzy logic PID control. Fuzzy logic PID control is a nonlinear control scheme with piecewise linear proportional, integral, and derivative gain to control the duty cycle of the system. Control of the duty cycle, in turn, controls the output voltage of the system. The fuzzy logic controller is designed to only implement proportional, integral, and derivative gains when they are appropriate to reduce the error signal of the system. Using fuzzy logic control, the time-domain response of the closed-loop system is improved with respect to the open-loop system. The overall speed of the system is also increased, as seen by the decrease of the settling time when the converter is connected to the power source. The system is also capable of fully rejecting disturbances by reducing the steady-state error to zero for a connection to a 12 V DC power source, a 1 A step change in load current, and 1 V step change in the power source voltage. In addition, the stability of the system is improved by reducing the overshoot/undershoot in all simulations. In all, the overall performance of the system is improved compared with the open-loop operating condition

Further investigation of the buck converter requires modeling and running a co-simulation between MATLAB/Simulink and circuit modeling software; either Synopsys Saber or Orcad PSpice. In addition, further investigation of the control of the buck converter required investigation into current-mode control and using fuzzy logic PID to regulate it. Finally, to test

the control and circuit designs, the circuit should be constructed from the corresponding components, a programmed DSP provide the fuzzy logic controller, and the entire system tested to ensure functionality.

## 8.1 Future Work

In future work, the system will focus on how to optimize the digital controller, which includes: reducing the number of the instructions to increase the achievable sampling frequency, implementing the synchronization of the sampling and switching cycle, tuning up the coefficients of the compensator and increasing the bandwidth of the low-pass filter to improve the transient response of the system.

A more complicated and nonlinear algorithm will be attempted in DSP to improve system performance, which is generally difficult to implement in analog circuits. This algorithm may include adaptive and predictive control or a control based upon efficiency peaking, thermal management and other factors.

The DSP can also play an important role in managing, monitoring and testing of the power system. DSP can be used to execute data acquisition, signal conditioning, filtering, spectral analysis and transient capture, and it has the capability to monitor and control systems concurrently. This is particularly useful in adaptive control because the controller can dynamically change the structure or parameters in real time in response to variations in system behavior. Testing capabilities built into power electronics systems are used to identify system parameters for automatic tuning of controller gains and to locate faults in the event of a failure. Such systems facilitate testing by performing a selected acquisition of data and recording the stimulated system responses.

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