# LOW FREQUENCY NOISE MODELING OF FERROELECTRIC THIN FILM TRANSISTOR

By

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Report on

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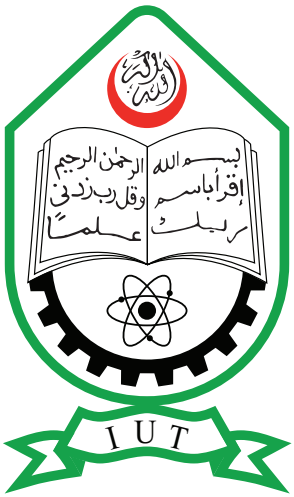


Department of Electrical and Electronic Engineering

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**LOW FREQUENCY NOISE MODELING OF FERROELECTRIC THIN FILM TRANSISTOR**

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# Declaration of Authorship

This is to certify that the work presented in this Thesis entitled, "Low Frequency Noise Modeling of Ferroelectric Thin Film Transistor", is the outcome of the research carried out under the supervision of Dr. Md. Masum Billah, Assistant Professor, Islamic University of Technology.

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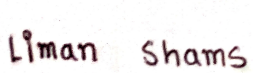


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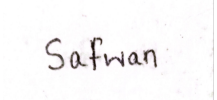


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# Acknowledgments

This book is dedicated to all our parents and family members, dedicated teachers, friends who endured the pain of tolerating us.

All the praise to Almighty Allah for the guidance and regards to our honorable supervisor for unwavering support.

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# List of Acronyms

| | |
|---|---|
| **1T1C** | 1 Transistor 1 Capacitor |
| **2T0C** | 2 Transistor 0 Capacitor |
| **2T1C** | 2 Transistor 1 Capacitor |
| **AI** | Artificial Intelligence |
| **CMOS** | Complementary Metal Oxide Semiconductor |
| **CO** | Course Outcome |
| **DRAM** | Dynamic Random Access Memory |
| **FeRAM** | Ferroelectric Random Access Memory |
| **FeTFT** | Ferroelectric Thin Film Transistor |
| **GUI** | Graphical User Interface |
| **HZO** | Hafnium Zirconium Oxide |
| **IGZO** | Indium Gallium Zinc Oxide |
| **IoT** | Internet of Things |
| **ITD** | Interface Trap Density |
| **K** | Knowledge Profile |
| **LFN** | Low Frequency Noise |
| **MFMIS** | Metal Ferroelectric Metal Insulator Semiconductor |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |
| **OBE** | Outcome Based Education |
| **PO** | Program Outcome |
| **RAM** | Random Access Memory |
| **TFT** | Thin Film Transistor |

# Abstract

Low-frequency noise (LFN) modeling and characterization in ferroelectric thin-film transistors (FeTFTs) is crucial for understanding and mitigating the effects of noise on device performance. This paper presents a comprehensive approach to LFN modeling that incorporates the unique characteristics of ferroelectric materials. Traditional TFT models are extended to include polarization-induced hysteresis, providing a more accurate representation of FeTFT behavior. Enhanced noise integration techniques are employed to account for various sources of low-frequency noise, including $1/f$ noise and thermal fluctuations. Parameter refinement for off current modeling is conducted to improve precision in predicting leakage currents. Additionally, advanced dynamic response models are developed to capture the timing and responsiveness of drain current under varying operational conditions. The convergence of memory window characteristics at peak gate voltages is improved to ensure reliable device operation. This work also refines the transfer characteristics equations to better reflect the low-frequency noise inherent to FeTFTs. Experimental results validate the proposed models, demonstrating significant improvements in noise characterization and device performance prediction. The findings contribute to the development of more reliable and efficient FeTFTs, suitable for applications in memory storage and low-power electronics. This thesis focuses on characterzing FeTFT, modeling the noise, as well as developing a Graphical User Interface (GUI) to simulate the memory window of the device.

# Chapter 1

# Introduction

As the world increasingly relying on cloud computing and memory-intensive applications such as AI, data centers, and IoT, the demand for efficient and scalable memory solutions has escalated. Traditional memory technologies face challenges of high latency, physical space limitations, and energy inefficiency. In response, Ferroelectric Thin Film Transistor (FeTFT) memory technology emerges as a transformative solution. FeTFTs offer significant advantages including high memory density in compact form factors, low latency for faster data access, non-volatility ensuring data integrity without constant power supply, enhanced energy efficiency, and prolonged lifespan due to their durability against repeated read/write cycles [1]. These attributes not only address current limitations but also support seamless integration into emerging technologies, making FeTFTs pivotal in meeting the burgeoning demands of modern computing infrastructures[2].

## 1.1 Low Frequency Noise

Low-frequency noise or 1/f noise (flicker noise) is a type of noise that is inversely proportional to the frequency. It has been observed in many electronic devices, including ferroelectric thin-film transistors (FeTFTs) [3]. The 1/f noise in FeTFTs is caused by carrier number fluctuation and grain boundary barrier fluctuation, which are both caused by carrier trapping/detrapping between the channel inversion carriers and the intra-grain traps within the Grain boundary depletion region for TFT.

### 1.1.1 Impact of Low Frequency Noise

Low-frequency noise (LFN) is a significant challenge in the realm of electronic devices, especially those that demand high sensitivity and precision [4]. It manifests as fluctuations in electrical current or voltage, following a 1/f noise spectrum. The implications of LFN are manifold and can adversely affect the performance of electronic devices. One of the primary repercussions is the degradation of the signal-to-noise ratio. This degradation can compromise the accuracy of the device, making it less reliable for precise measurements or computations. Another consequence of LFN is increased power consumption. The presence of LFN can cause a device to use more power than necessary, leading to inefficiencies and potentially shortening the device's lifespan. Lastly, LFN can lead to potential errors or failures in device operation. These errors can range from minor inaccuracies to major malfunctions, depending on the severity of the noise and the specific

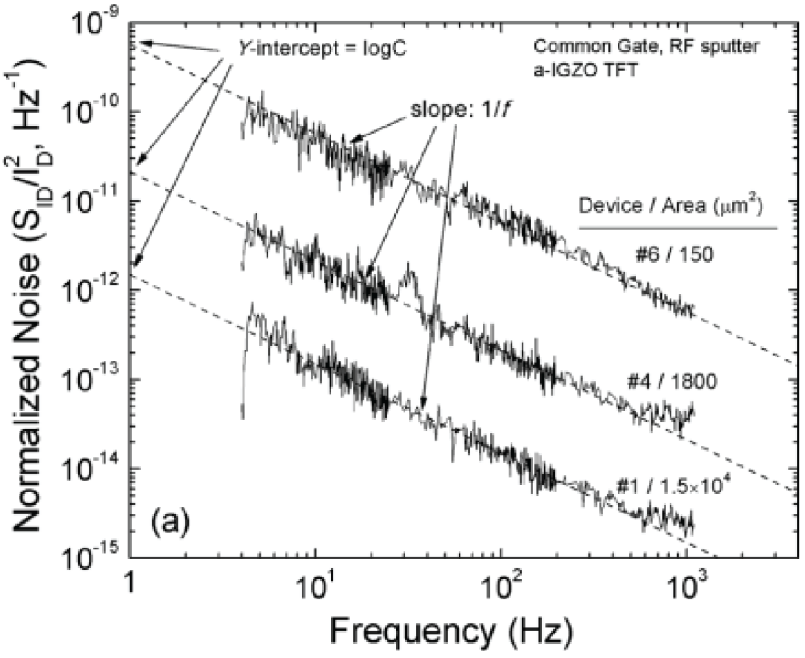


Figure 1.1: Low Frequency Noise

application of the device. Therefore, understanding and mitigating LFN is crucial in the design and operation of electronic devices.

## 1.2 Study of LFN in FeTFT

Ferroelectric Thin Film Transistors (FeTFTs) are a promising technology in the field of non-volatile memory devices .Their special qualities allow them to be used in a wide range of settings. FeTFTs' properties related to Low-frequency noise (LFN) are among its most important features. Models to explain LFN in thin-film transistors can be developed using LFN, which can offer important insights into the electrical conduction mechanisms in these devices.

LFN measurements can also be used to analyze the conduction mechanism and evaluate the device/material reliability, which is crucial for improving the performance and longevity of the devices. The models used to describe LFN in thin film transistors stem from those developed for $1/f$ noise in metal-oxide-semiconductor field-effect transistors (MOSFETs). These models have been adapted to take into account the effects of the non homogeneous conducting channel.

## 1.3 Different Aspects of the study

The study of Low-Frequency Noise (LFN) modeling in Ferroelectric Thin Film Transistors (FeTFTs) encompasses several aspects. It begins with understanding the electrical conduction mechanisms in thin film transistors using LFN, which forms the basis for developing models to describe LFN in these devices. The reliability of the device and the materials used in its construction are evaluated using LFN measurements. The effects of the nonhomogeneous conducting channel on LFN in thin film transistors are also taken

into account. In inverted staggered structures, the noise associated with access resistances is a particular aspect of LFN in thin film transistors. Each of these aspects plays a crucial role in understanding, designing, and optimizing the performance of FeTFTs, providing valuable insights into the device's operation, reliability, and the effects of various factors on its performance.

Furthermore, the application of advanced analytical techniques deepens the comprehension of Low-Frequency Noise (LFN) in FeTFTs. Spectral analysis enables the identification of various noise components, such as $1/f$ noise and generation-recombination noise, providing a comprehensive understanding of noise sources and their effects. Time-domain analysis reveals transient noise behaviors, offering insights into the FeTFTs' temporal stability and dynamic response under different operating conditions. By extracting specific noise parameters, like the Hooge's parameter, researchers can quantify the contributions of different noise sources, facilitating comparisons across diverse materials and device architectures. Statistical methods, such as Monte Carlo simulations, model the variability in noise characteristics, which is crucial for evaluating device robustness and reliability. As FeTFTs are miniaturized, understanding how scaling affects LFN is essential, as smaller devices may become more sensitive to fabrication variations and material defects. Enhancing material and interface quality by minimizing defects and optimizing charge transport can significantly lower noise levels. Additionally, investigating alternative ferroelectric and channel materials with lower intrinsic noise characteristics can further improve FeTFT performance. Environmental factors, such as temperature and humidity, also impact LFN behavior, requiring thorough investigation to ensure reliable device operation under various conditions.

## 1.4 Background and Motivation

Low-frequency noise (LFN) poses significant challenges to electronic devices, particularly those requiring heightened sensitivity and precision, manifesting as fluctuations in electrical current or voltage following a 1/f or flicker noise spectrum. LFN's repercussions include degraded signal-to-noise ratios, increased power consumption, and potential errors or failures in device operation. Ferroelectric thin film transistors (FeTFTs) show promise in electronic systems, leveraging ferroelectric materials for enhanced functionality, memory capabilities, and improved switching. Yet, the intrinsic LFN characteristics of FeTFTs are not fully understood, necessitating meticulous exploration. LFN in FeTFTs is influenced by material properties, device geometry, operating conditions, and the complexities of ferroelectric switching behavior, impacting memory and switching performance, as well as overall system functionality and reliability.

In contrast, conventional memory devices like dynamic random access memory (DRAM) and flash memory operate on mechanisms distinct from FeTFTs, with unique advantages and disadvantages in speed, density, endurance, volatility, and scalability. However, conventional memory devices are not immune to LFN-related challenges, constraining their performance and reliability [5].

Hence, a compelling need exists to develop a thorough and accurate model of LFN in FeTFTs grounded in physical mechanisms and empirical data. Such a model holds potential for predicting and optimizing FeTFT noise performance and applications. Additionally, it enables a comparative analysis of LFN traits in FeTFTs against other memory devices, providing insights into the advantages and challenges of deploying FeTFTs for

memory and logic applications.

To deepen our understanding of LFN in FeTFTs, it's essential to utilize advanced characterization methods and simulation tools. Techniques such as low-frequency noise spectroscopy, scanning probe microscopy, and high-resolution electron microscopy enable detailed examination of noise sources at microscopic and atomic scales. Simulation tools like multi-scale modeling and finite element analysis allow us to model the complex interactions within FeTFTs, providing critical insights into noise behavior under various operating conditions. These methods help identify and mitigate key noise sources, supporting the optimization of FeTFT design and material choices. Collaboration between academia and industry is crucial for developing standardized testing protocols and benchmarking methods for LFN in FeTFTs. Such collaborations ensure that research findings are effectively translated into practical applications, improving the reliability and performance of FeTFT-based systems. By combining experimental characterization, theoretical modeling, and collaborative research efforts, we can develop innovative solutions to address LFN challenges in FeTFTs, positioning them as strong contenders against traditional memory technologies.

# Chapter 2

# Overview of Memory Transistors

Ferroelectric Thin Film Transistor (TFT) based memory has been a subject of interest for researchers and technologists for several decades. The evolution of this technology can be traced back to the 1960s, when the development of semiconductor integration technology sparked interest in applying ferroelectric thin films to non-volatile memory devices.

The key to the success of these memory devices lies in their ability to retain data even after a power failure, making them an integral part of modern electronic information technology. As the electronics industry evolves, devices continue to shrink in size, operate at lower voltages, and consume less power, making it difficult for current charge-trapping-based flash memory technology to meet market demand for smaller sizes and lower operating power consumption.

One of the most significant breakthroughs in this field came with the discovery of ferroelectric properties in fluorite-structure oxides such as hafnium oxide ($HfO_2$) and zirconia3. These materials have various advantages such as Si-based complementary metal oxide semiconductor-compatibility, matured deposition techniques, a low dielectric constant and the resulting decreased depolarization field, and stronger resistance to hydrogen annealing.

In recent years, the focus has shifted towards the study of current ferroelectric materials, with particular emphasis on the properties of Zr, Al, and Si-doped $HfO_2$ devices. These devices have shown promising results, with FeRAM (Ferroelectric Random Access Memory) being the only new memory device with the most mature technology available on the commercial market. It has the advantages of extremely low operating voltage, ultra-fast erasure speed, good radiation resistance, and excellent repeated erasure capability.

The future of ferroelectric thin film transistor (FeTFT)-based memory devices is bright, with ongoing research focusing on innovative nanostructures and hybrid materials. Scientists are exploring the potential of 2D ferroelectric materials and their integration into FeTFTs, aiming for enhanced scalability and performance. Additionally, hybrid ferroelectric materials, blending organic and inorganic components, are opening pathways for flexible electronics applications, leveraging both mechanical flexibility and superior electronic properties.

Advanced manufacturing techniques like atomic precision manufacturing and nanolithography are also playing pivotal roles in pushing the boundaries of miniaturization and

efficiency for these memory devices. These methods enable the creation of precisely controlled nanostructures, which can significantly improve FeTFT performance and reliability. Interdisciplinary research efforts across materials science, electrical engineering, and computational modeling are further refining ferroelectric materials' design, tailoring their properties to meet specific memory technology requirements.

Simultaneously, integrating FeTFTs with emerging technologies such as IoT and AI holds promise. Such integrations capitalize on ferroelectric memory's advantages—low power consumption and high-speed operation—to develop intelligent and energy-efficient electronic systems. This convergence underscores FeTFT-based memory's evolution, adapting to meet the needs of an increasingly digital and interconnected global landscape.

## 2.1 Memory Architecture

### 2.1.1 The Principle of DRAM architecture

Dynamic Random-Access Memory (DRAM) is classified as volatile memory due to its inherent characteristic of requiring a continuous power supply to maintain the integrity of the stored information[6]. The data within DRAM is preserved through a process of constant refreshment, which occurs while the system is powered. However, in the event of a power disruption, the information stored in DRAM is rapidly lost, as the memory cells are unable to retain data without electrical power[7]. This transient nature of data retention necessitates the use of DRAM in conjunction with non-volatile memory solutions for persistent data storage with faster access time.

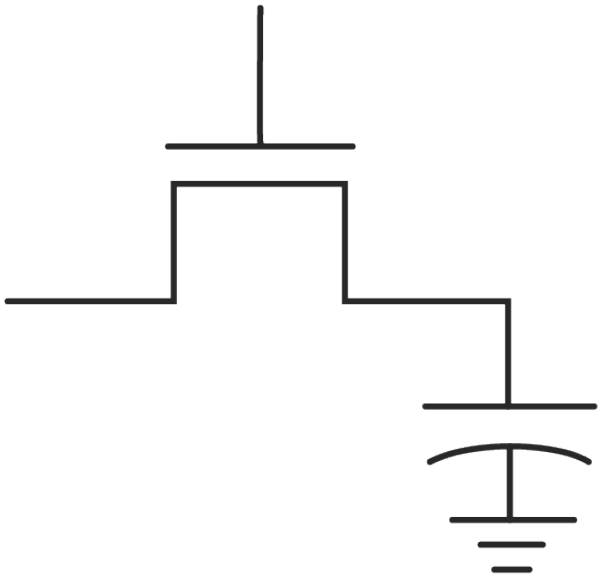

Figure 2.1: Unit Cell of DRAM (1T1C)

### 2.1.2 2T1C and 2T0C DRAM

In the context of DRAM cell architectures, "2T1C" and "2T0C" refer to two distinct configurations. The "2T1C" configuration denotes a memory cell with two transistors and one capacitor, while the "2T0C" configuration represents a cell with two transistors and zero capacitors.[8]

The “2T1C” cell is a variation of the traditional “1T1C” DRAM cell [9], which consists of one transistor and one capacitor. In a “2T1C” cell, the addition of a second transistor allows for improved isolation between the capacitor that stores the charge and the bitline used for reading the data. This results in better retention characteristics and reduced leakage currents[10].

On the other hand, the “2T0C” DRAM cell architecture is a novel approach that eliminates the need for a storage capacitor altogether[11]. Instead, it utilizes the parasitic capacitance of the read transistor as the storage element. This innovative design has been made possible by indium-gallium-zinc-oxide thin-film transistors (IGZO-TFTs), which are known for their very low off-currents. The absence of a storage capacitor in the “2T0C” configuration allows for a smaller cell footprint and the potential for stacking individual cells, paving the way for high-density 3D-DRAM memories.[8]

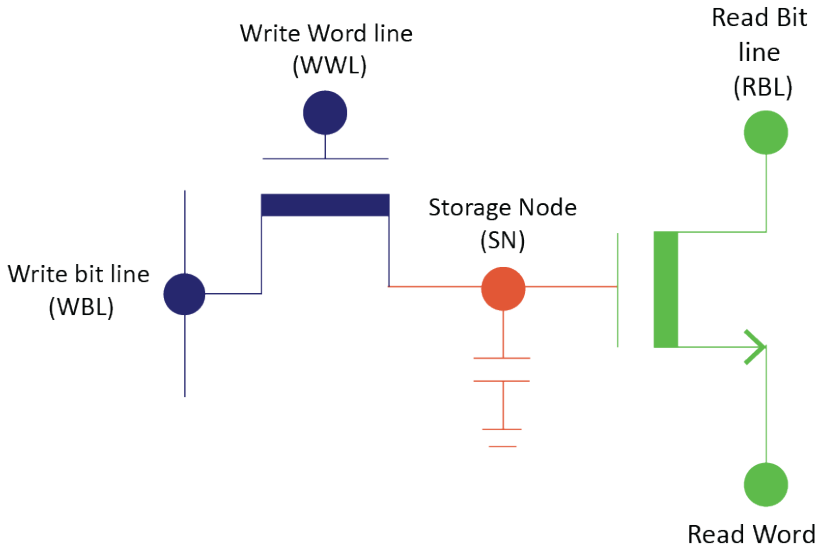


Figure 2.2: 2T1C Memory Cell

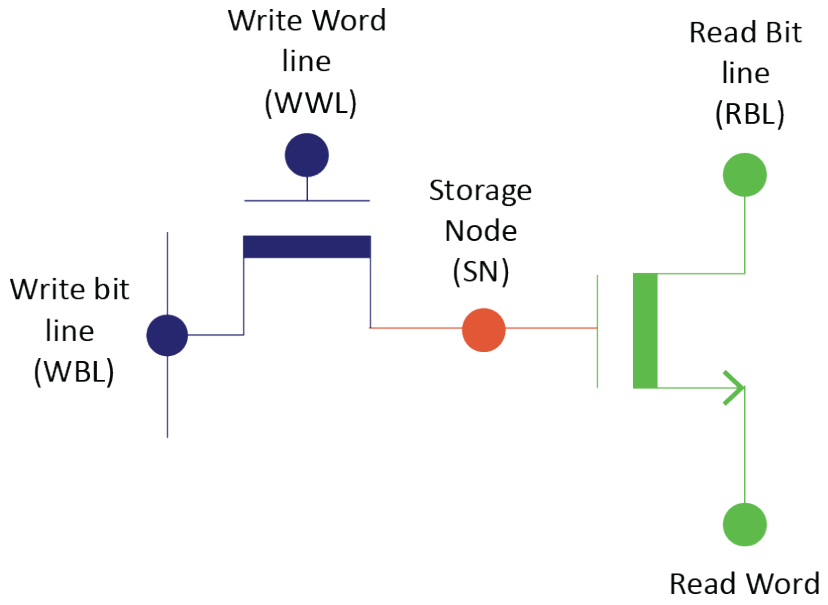


Figure 2.3: 2T0C Memory Cell

## 2.2 Assessments on the Architectures

### 2.2.1 Advantages of 2T1C

- **Higher Noise Margin:** The storage capacitor provides a larger charge storage region, enhancing robustness against electrical noise [12].
- **Simplified Sensing Circuitry:** Direct sensing of the charge on the capacitor simplifies the readout circuitry [13].

### 2.2.2 Disadvantages of 2T1C

- **Larger Cell Size:** The inclusion of a capacitor increases the overall size of the memory cell [13].
- **Complex Manufacturing:** The process of integrating a capacitor with the transistors can be more complex.

### 2.2.3 Advantages of 2T0C

- **Smaller Cell Size:** Eliminating the capacitor can lead to a smaller cell size and higher density [14].
- **Simplified Manufacturing:** Fewer components may simplify the manufacturing process.

### 2.2.4 Disadvantages of 2T0C

- **Increased refresh costs:** As DRAM cells shrink, they require more frequent refreshes due to decreasing parasitic capacitance for individual, which consumes more energy and reduces efficiency.
- **Retention time variation:** Over time, the ability of a DRAM cell to retain data becomes less predictable, which can lead to data loss or the need for additional error-checking mechanisms, requiring complex circuitry and fabrication[15].
- **Complex Sensing Mechanisms:** The smaller amount of charge requires more complex sensing mechanisms.
- **Limited Scalability:** As technology nodes shrink, maintaining performance becomes more challenging without a dedicated capacitor.

## 2.3 Parasitic Capacitance in Transistors

Parasitic capacitance in Transistors refers to the unintended capacitance that exists in the device due to the physical structure and layout of the transistor. This parasitic capacitance can affect the performance of the transistor, including its speed, power consumption, and functionality [16].

In the context of FeTFTs, one of the key parasitic capacitances is associated with the gate structure. The ferroelectric material in the gate forms a capacitor with the semiconductor channel. This capacitance is essential for the operation of the transistor, as it allows the gate voltage to modulate the channel conductivity. However, due to the physical layout

of the transistor, there can be additional unwanted capacitance between the gate and other parts of the transistor or the circuit[17].

Another significant aspect of parasitic capacitance in FeTFTs is related to the use of ferroelectric materials. These materials can exhibit negative capacitance, a phenomenon where the voltage across the capacitor decreases with increasing charge. This property can potentially be used to overcome the fundamental energy-efficiency limits of conventional transistors[18].

However, the presence of parasitic capacitance can complicate the behavior of the device and needs to be carefully considered in the design and operation of FeTFTs[19]. It's important to note that while parasitic capacitance is generally undesirable, in some cases, it can be used to advantage, such as in the stabilization of the negative capacitance state.

Parasitic capacitance in Transistors arises from gate-source/drain electrode overlaps and dielectric properties, affecting charge transfer. In 2T0C DRAM, it replaces the storage capacitor, reducing cell size and power usage, and enhancing retention, crucial for memory scaling in advanced computing applications [20].

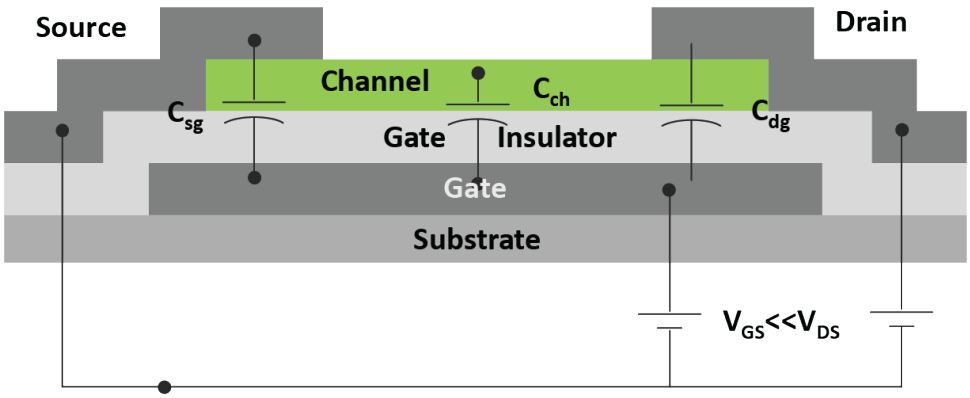


Figure 2.4: Parasitic Capacitance in TFT

## 2.4 Thin Film Transistor (TFT)

A Thin Film Transistor (TFT) is a specific type of field-effect transistor that is made by depositing thin films of an active semiconductor layer as well as the dielectric layer and metallic contacts over a supporting substrate. A key characteristic of TFTs is their thin form factor, which allows them to be used in applications where space is at a premium, such as in high-density stacking configurations.

When it comes to memory applications, the gate interface of the TFT can be modified with a ferroelectric material to create a Ferroelectric Thin Film Transistor (FeTFT). Ferroelectric materials have unique properties, including the ability to retain their polarization state even when the electric field is removed. This makes them well-suited for non-volatile memory applications, where data must be retained even when power is not supplied [21].

Hafnium-based ferroelectric materials, such as hafnium oxide (HfO2), are often used in FeTFTs due to their low power consumption, high operational speed, and compatibility with complementary metal–oxide–semiconductor (CMOS) technology [22]. These mate-

rials can be scaled down to a 10-nm dimension using a vertical structure, making them suitable for high-density three-dimensional memory applications [23] [24].

Moreover, the use of ferroelectric materials in TFTs opens up possibilities for diverse computing architectures, such as neuromorphic computing with analog characteristics or logic-in-memory computing with digital characteristics, through high integration.

## 2.5 Ferroelectric Thin-Film Transistor (FeTFT)

These are a type of transistor that uses a ferroelectric material in their gate stack [25]. They are considered promising candidates for future non-volatile memory devices due to their low power consumption, high operational speed, and compatibility with complementary metal–oxide–semiconductor (CMOS) technology.

### 2.5.1 Ferroelectric Behavior

- FeTFTs utilize a ferroelectric material in their gate stack. This material is key to the operation of the transistor.
- The ferroelectric layer exhibits spontaneous polarization, which means it can naturally create an electric polarization without an external electric field [26].
- This polarization can be switched between two stable states, often referred to as "up" and "down". This switching is typically achieved by applying an external electric field.
- The state of the polarization serves as the memory element. In other words, each state ("up" or "down") can represent a bit of information (0 or 1), allowing the transistor to store data.

### 2.5.2 Hafnium–zirconium oxide (HZO)

This is a type of ferroelectric material that is often used in FeTFTs. HZO has several advantages, including its ability to maintain ferroelectricity even at a thickness of 10 nm [27], excellent insulating properties, and suitability for use as gate oxides in FeTFTs. It's also compatible with CMOS technology, which makes it a good fit for integration into modern electronic devices [23] [24] .

In conclusion, FeTFTs, with their unique ferroelectric behavior and the use of materials like HZO, offer a promising path towards efficient, high-performance memory devices.

# Chapter 3

# Methodology

## 3.1 Working Principle of FeTFT

One of the key materials used in the construction of FeTFTs is Hafnium–Zirconium Oxide (HZO). HZO is a high-k dielectric material that exhibits strong ferroelectricity, even at nanometer thicknesses [28] [29]. This makes it an ideal choice for use in FeTFTs, where the ability to retain polarization in the absence of an electric field is crucial.

The active layer channel in these transistors is often made from Indium Gallium Zinc Oxide (IGZO) [17]. IGZO is a compound semiconductor material that has higher electron mobility and carrier concentration compared to traditional amorphous silicon. This results in improved transistor performance, including faster switching speeds and lower power consumption [30].

The operation of an FeTFT can be understood by examining its behavior under different gate voltages. When the gate voltage is off and a voltage source is connected to the drain and source, current will flow due to the active layer channel. This is a fundamental characteristic of a depletion type transistor.

As the gate voltage is swept to a positive value, negative carriers (electrons) are attracted and gather around the vicinity of the dielectric ferroelectric interface. Simultaneously, positive carriers in the ferroelectric layer get repelled and gather near the dielectric and active channel layer interface. As the active channel has excess electrons which flow from source to drain, some of the electrons will recombine with the holes. This results in a reduction in the size of the active layer path and a decrease in the current flow as the gate voltage increases. A significant amount of gate-drain voltage ($V_{GD}$) will substantially cut off the current flow.

If we then sweep the gate-source voltage ($V_{GS}$) in the negative direction, a sudden increase in the current flow is observed. This is because the recombined charges will be broken down, while more and more electrons will be accumulated in the channel-ferroelectric interface. This accumulation of electrons effectively lowers the threshold voltage of the transistor, allowing it to turn on at a lower gate voltage.

Finally, if we trace back the $V_{GS}$ again, we will find a hysteresis characteristic caused by the ferroelectric material of the FeTFT. This hysteresis loop is a direct result of the polarization reversal in the ferroelectric material, and it is this property that allows FeTFTs to be used in non-volatile memory applications.

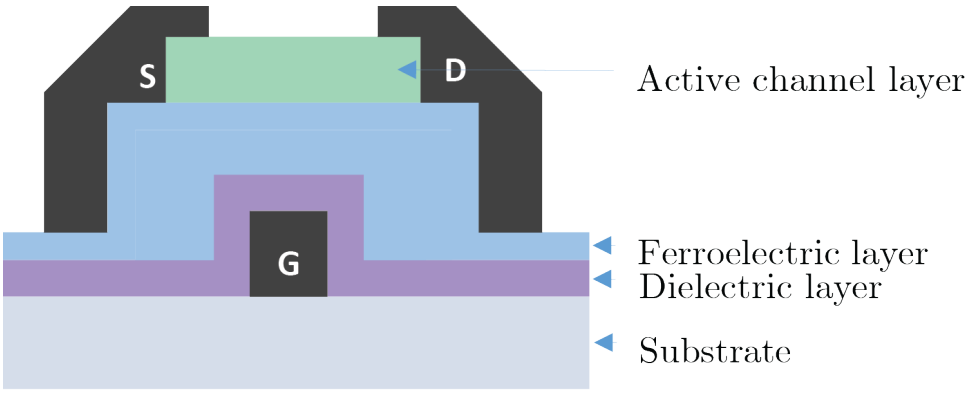


Figure 3.1: FeTFT Device Structure

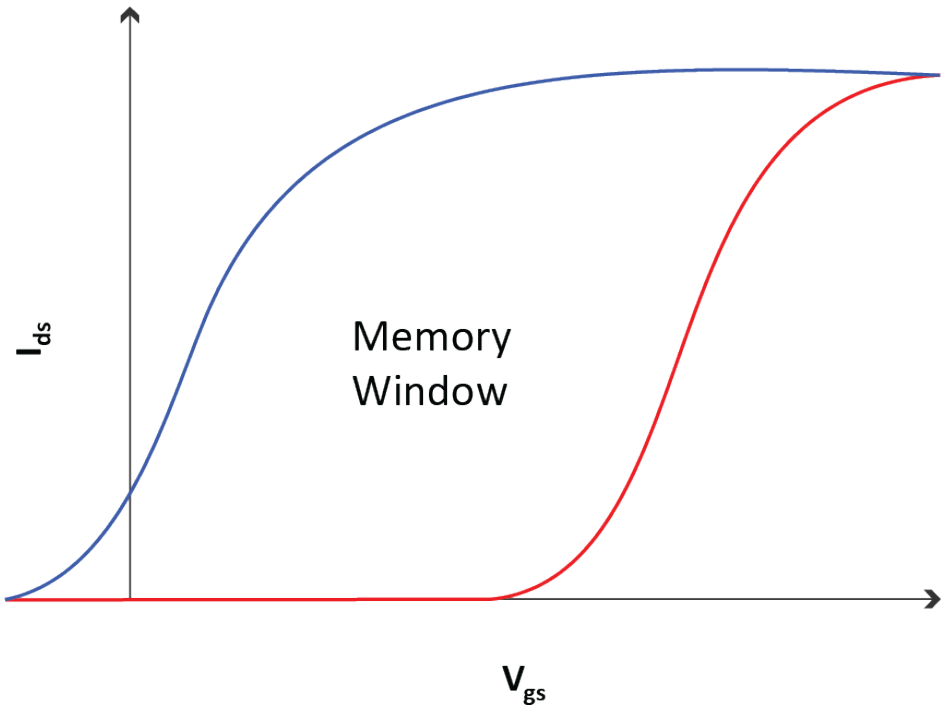


Figure 3.2: FeTFT Memory Window

## 3.2 Relevant Software

- MATLAB/Simulink

  - Graphical User Interface Development which can be interacted by inputting various parameters of the FeTFTs and

  - Modeling Transfer Characteristics of the thin film transistor

  - Modeling Output Characteristics of the thin film transistor

  - Off Current modelling and evaluation.

  - Hysteresis Analysis

  - Noise modeling

## 3.3 Data Collection

Experimental data required for further exploration was acquired from **Advanced Display Research Center(ADRC)** at **Kyung Hee University**. The experimental data represents the Transfer Characteristics of FeTFT.


Thin Film Transistor
Display Center

경희대학교
KYUNG HEE UNIVERSITY

## 3.4 Theory

### 3.4.1 Transfer Characteristics

The transfer characteristics equation of a Thin-Film Transistor (TFT) describes how the drain current ($I_D$) flowing through the transistor varies with the gate-source voltage ($V_{GS}$) and drain-source voltage ($V_{DS}$). Typically, in an ideal TFT, the transfer characteristics can be expressed using a square-law model for the saturation region [31].

Linear Region:

$$I_D = \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH}\right) V_{DS} - \frac{1}{2} V_{DS}^2 \qquad ; V_{DS} < V_{GS} - V_{TH} \tag{3.1}$$

Saturation Region:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2 \qquad ; V_{DS} > V_{GS} - V_{TH} \tag{3.2}$$

Where,

$\mu$ = Carrier Mobility
$C_{ox}$ = Oxide Capacitance
$W$ = Channel Width
$L$ = Channel Length
$V_{TH}$ = Threshold Voltage
$V_{GS}$ = Gate Voltage

This equation describes the quadratic relationship between drain current and gate-source voltage in the saturation region of operation, where the transistor behaves as a voltage-controlled current source. Understanding and accurately modeling the transfer characteristics equation is crucial for designing and optimizing TFT-based circuits and systems, ensuring desired performance and functionality in various electronic applications.

### 3.4.2 Trap Density Approximation Model

The threshold voltage ($V_{TH}$) is a crucial parameter in Thin-Film Transistor (TFT) research, particularly in memory applications, where precise VTH control is essential for defining the memory window. This window represents the range of gate voltages that facilitate reversible conductivity switching, crucial for non-volatile memory devices. Interface Trap Density (ITD) significantly influences VTH and shapes the memory window by governing the density of electronic states at the semiconductor-insulator interface in TFT structures. ITD arises from imperfections, defects, and dangling bonds at this interface, which impact charge carrier trapping and mobility within the semiconductor channel. The energy range over which these traps operate determines their ability to capture and release charge carriers, thereby affecting transistor behavior and memory performance. Manipulating ITD through material engineering and interface optimization allows for tailored adjustments to $V_{TH}$, ensuring the reliable operation and longevity of TFT-based memory devices. Advancements in fabrication techniques and dielectric materials further enhance the management of ITD, improving the stability and endurance of the memory window in TFTs engineered for next-generation memory applications [31].

$$\Delta V_{TH} = \frac{Q_{it}}{C_{ox}}$$
$$\Delta V_{TH} = \frac{q \cdot \Delta E \cdot D_{it}}{C_{ox}} \tag{3.3}$$

Where,

$q$ = Elementary Charge
$C_{ox}$ = Oxide Capacitance
$\Delta E$ = Energy Range over which the traps are active*
$D_{it}$ = Interface Trap Density
$V_{TH}$ = Threshold Voltage

**Energy range over which the traps are active basically refers to the energy levels in band gap where these traps are active and can capture and release charge carriers.*

### 3.4.3 Approximation Based On Channel Dimensions

In the domain of TFTs, it's essential to grasp how the Threshold voltage ($V_{TH}$) varies with channel dimensions for optimal device performance. The equation below is pivotal here [32].

$$\Delta V_{TH} = \frac{1}{2}\left(\frac{C_{ox}}{W} \cdot \frac{L}{W}\right) \tag{3.4}$$

This equation illustrates that as the channel length $L$ increases, $\Delta V_{TH}$ decreases in a straightforward manner, indicating reduced sensitivity to trap density variations at longer lengths. Conversely, with increasing channel width $W$, $\Delta V_{TH}$ decreases more significantly, showing a stronger impact on $V_{TH}$ due to increased capacitance between the gate and channel [33].

Understanding these relationships is crucial in TFT design. Engineers can utilize this equation to adjust $V_{TH}$ based on specific application needs, optimizing device performance in terms of speed, power consumption, and reliability. By effectively managing $L$ and $W$, TFTs can be engineered to deliver superior electrical performance and operational efficiency across a range of electronic applications.

### 3.4.4 Noise Model

Hooge's model [34] provides a theoretical framework for explaining low-frequency noise, particularly $1/f$ noise, observed in electronic devices like transistors such as TFTs. It states that the noise spectral density ($S_{ID}$) is inversely proportional to frequency ($f$), given in the equations below,

Here, alpha ($\alpha$) represents the Hooge's parameter, a dimensionless constant reflecting various physical and geometrical properties of the device.

The occurrence of $1/f$ noise arises from fluctuations in carrier number and mobility within the semiconductor material and at its interfaces. These fluctuations are caused by defects, traps, and imperfections in the material's crystalline structure. At higher frequencies, the noise spectral density $S_{ID}$ decreases, indicating lower noise amplitude, whereas it increases at lower frequencies [35].

The significance of Hooge's model lies in its ability to quantify and characterize inherent noise sources in electronic devices. By analyzing $1/f$ noise, engineers can assess semiconductor material quality, optimize fabrication processes, and enhance device performance in applications sensitive to noise levels, such as low-power electronics, sensors, and communication systems.

Practically, understanding Hooge's model involves experimental measurement of noise spectra across different frequencies, correlating these findings with device parameters and operational conditions. This approach guides engineers in minimizing noise effects, improving device reliability, and achieving better overall performance.

This is the equation that helped us develop the noise profile based on $V_{TH}$. There are several models that can be used to describe and analyze low frequency noise of $1/f$ noise other than Hooge's model. In the equation the Hooge's constant is taken to be 0.2; standardized for IGZO. $S_{ID}/I_D^2$ is basically normalized Power Spectral Density helps us compare the noise property of different devices or the same device under different biasing conditions [3].

According to Hooge's Model,

Linear Region:

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H}{f}\frac{q}{C_{ox}WL}\frac{1}{V_{GS}-V_{TH}} \tag{3.5}$$

Saturation Region:

$$\frac{S_{ID}}{I_{Dsat}^2} = \frac{\alpha_H}{f}\frac{2q}{C_{ox}WL}\frac{1}{V_{GS}-V_{TH}} \tag{3.6}$$

# Chapter 4

# Results and Future Improvements

## 4.1 Simulation Results

### 4.1.1 Plot of Acquired Data

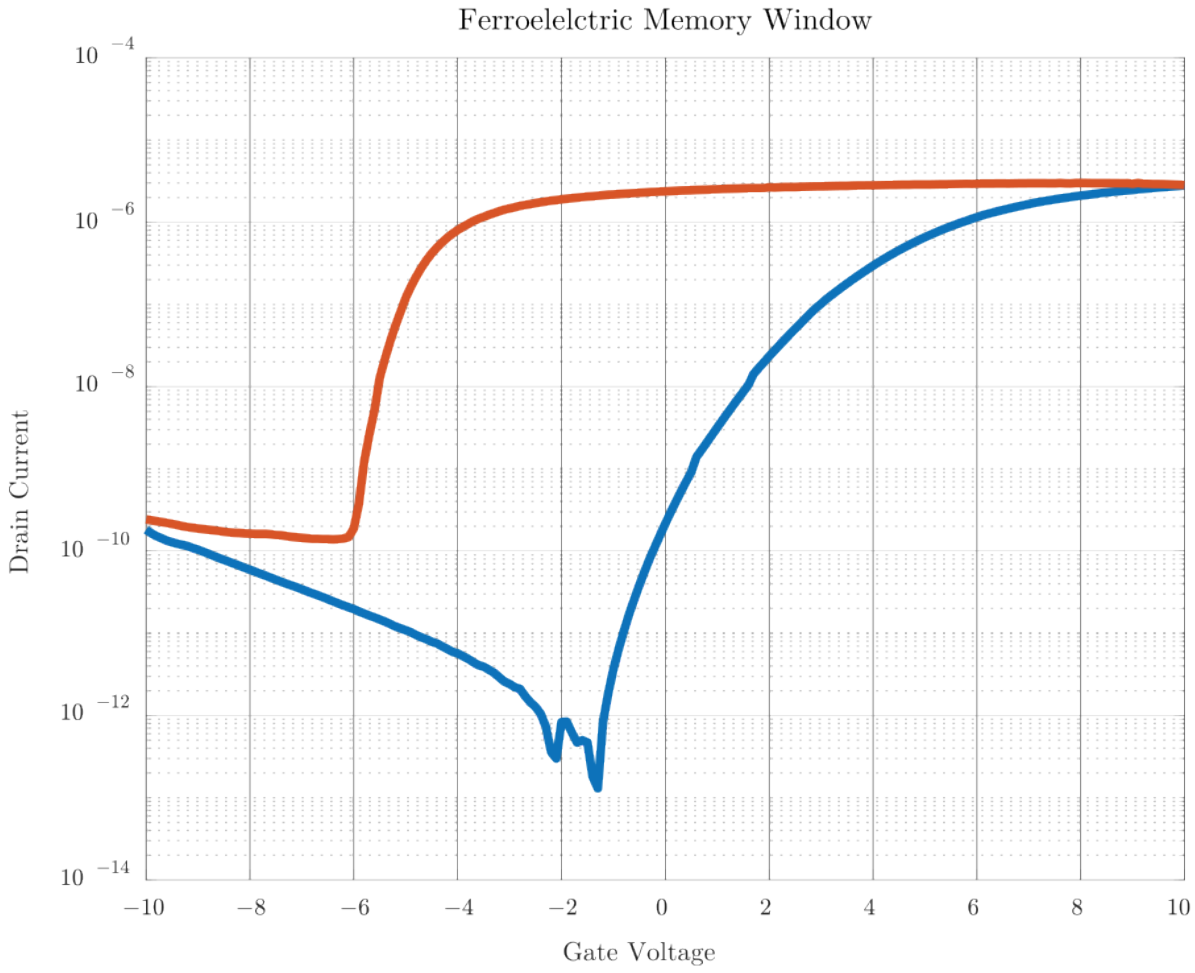


Figure 4.1: Graphical Representation of experimental data acquired from ADRC

### 4.1.2 Plot of Simulation

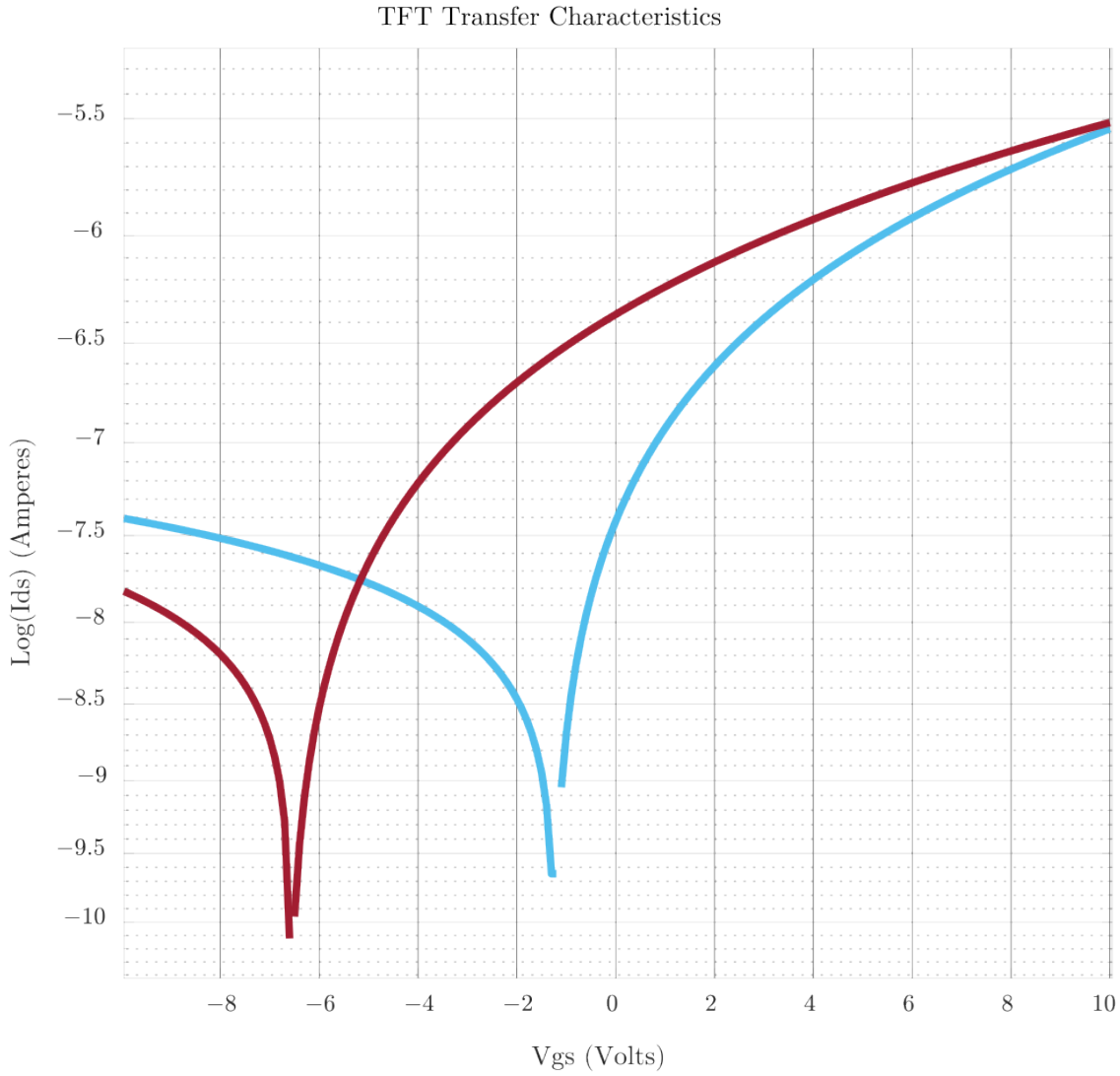


Figure 4.2: Graphical Representation of theoretical Transfer Characteristics Equation

For the initial generation of the plot, we used standard values for the parameters to match it with the collected practical data as accurately as possible. For the generation of plot in Figure 4.2

$$\begin{aligned} \mu &= 10 \times 10^{-}3\ m^2V^{-1}s^{-1} \\ C_{ox} &= 900\ nF \\ W &= 50\ \mu m \\ L &= 10\ \mu m \end{aligned}$$

One of the plots for the transfer characteristics equation is always kept constant $V_{GS}$ at $-1.3V$ represented by the blue lines in the figure 4.2 and is swept from $-10V$ to $10V$ for $V_{DS}$ in order to generate the curve. The red line that holds the value around $-6.3V$ is generated through the Interface Trap Density equation where the value of the

density was $10^14\ eV^{-1}cm^{-2}$. The range of energy for trap density is kept at 0.3 $V$. The comparison with the practical data is shown in Figure 4.3. The comparison provides a clear distinction. Although the with of the memory window is quite identical the practical model does not fully represent the experimental data in terms of other aspects.

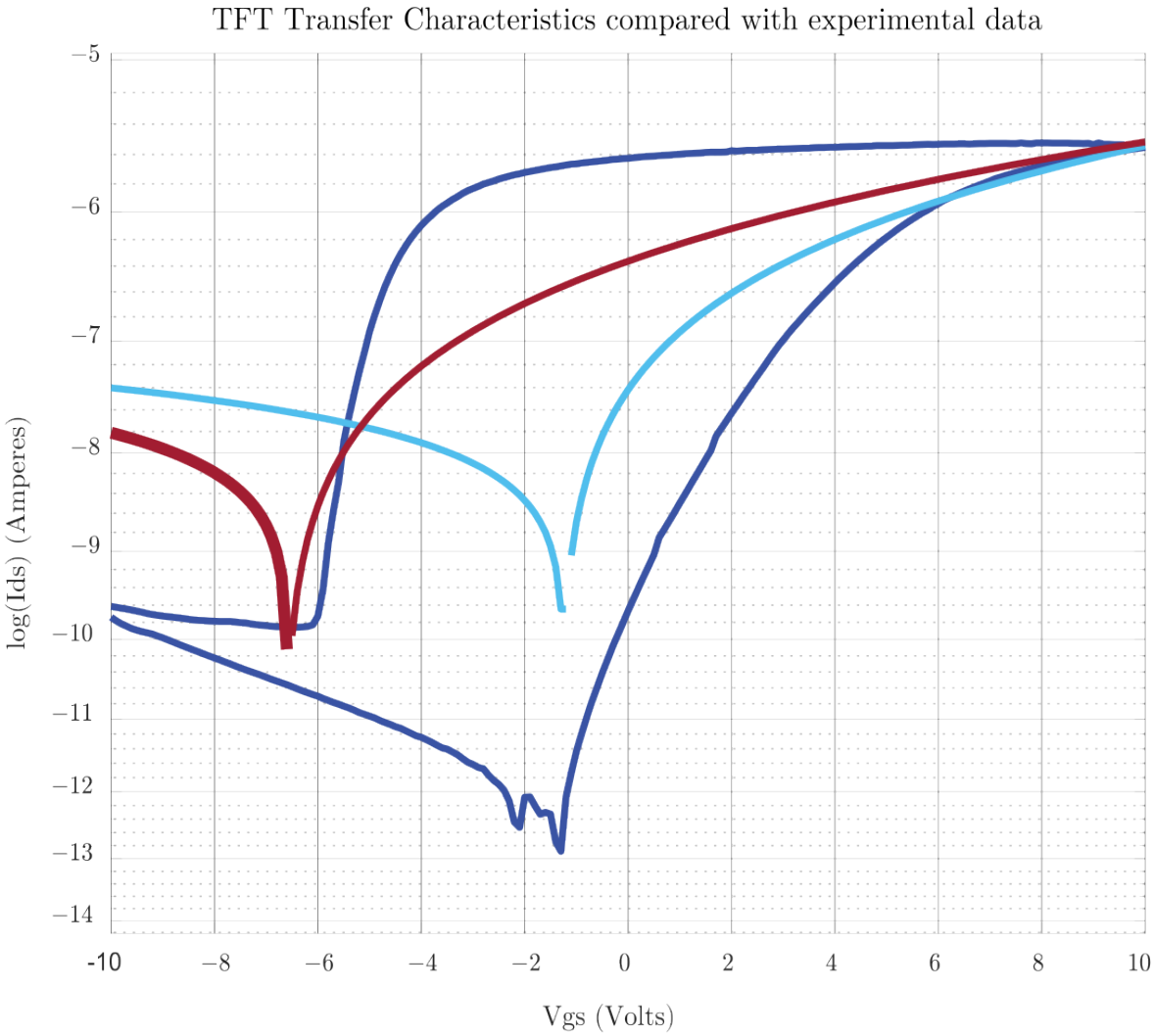


Figure 4.3: Comparison between theoretical and experimental data

Afterwards the noise model was implemented to achieve the noise profile depicted in figure 4.4 The three lines represent three different threshold voltages; top most line is for the highest and lower lines are for lower values of threshold voltage.

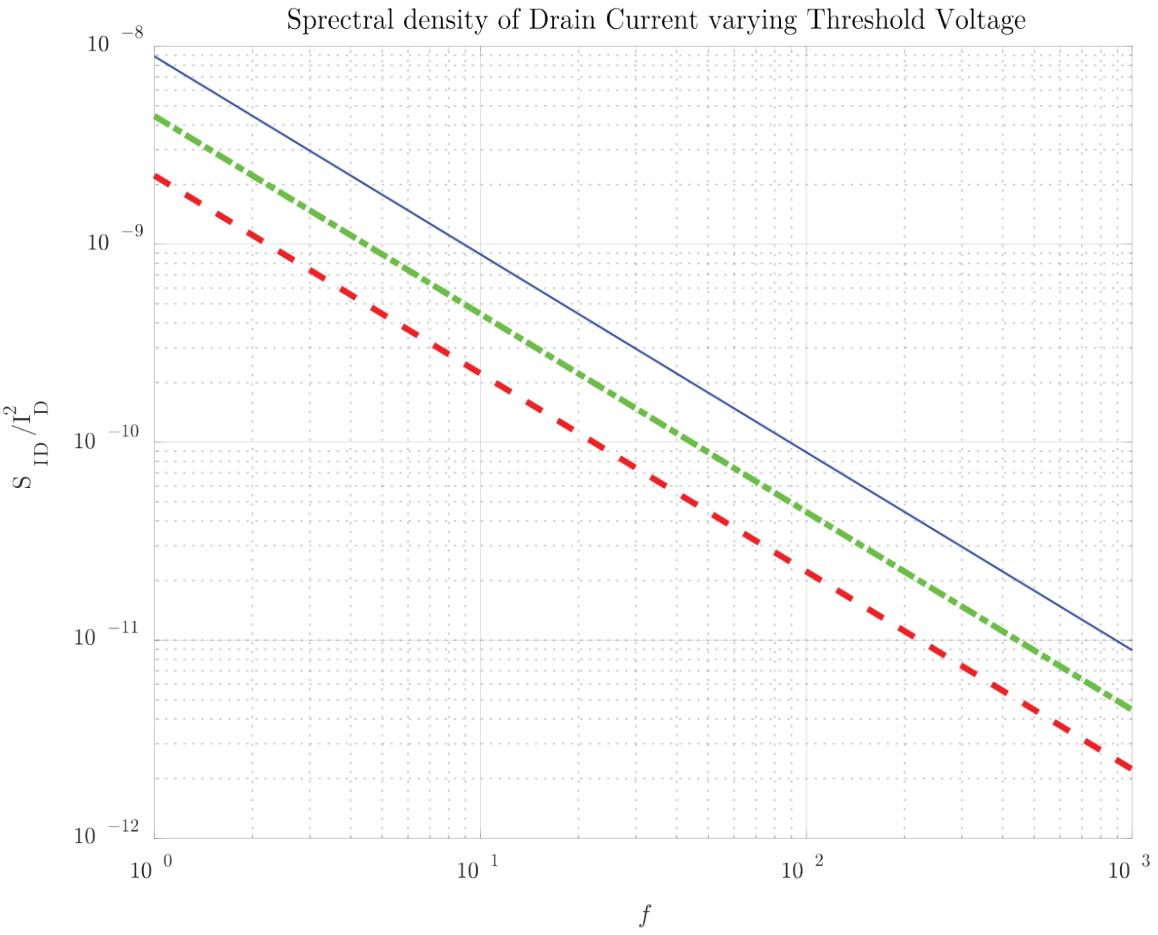


Figure 4.4: Graphical Representation of Noise Profile Plotted using Hooge's Model

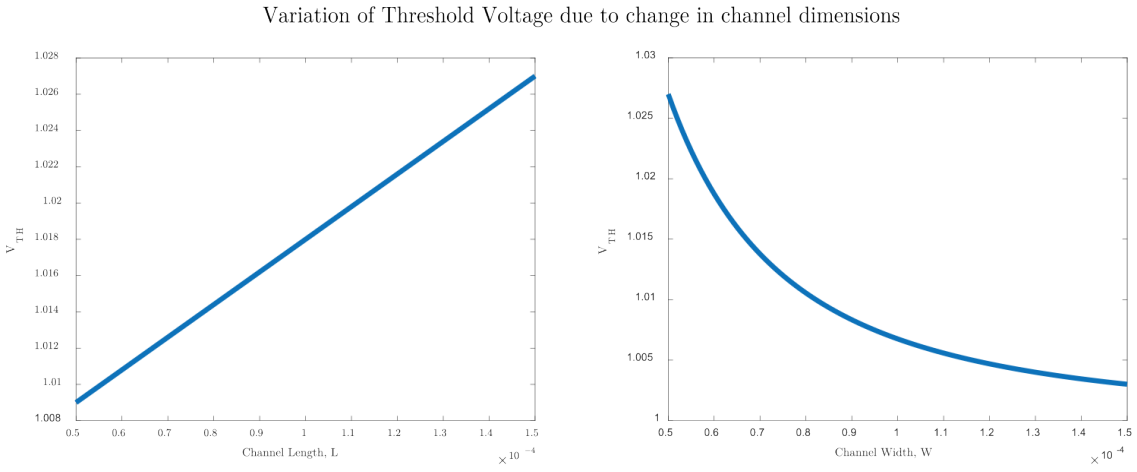


Figure 4.5: Graphical Representation of variation of Threshold Voltage with respect to channel dimensions.

## 4.2 Graphical User Interface Implementation

Once the basic development of our work is done, we attempted to build a simulator using MATLAB GUI as shown in figures 4.6 and 4.7 . Our simulator has two modes, where in the first mode which can be seen in figure 4.6 as per the value of Interface Trap Density the memory window will be generated. For the second mode, we directly provide the width of the memory window we require and the simulator will provide a graphical representation along with the noise profile for the resultant threshold voltage as shown in Figure

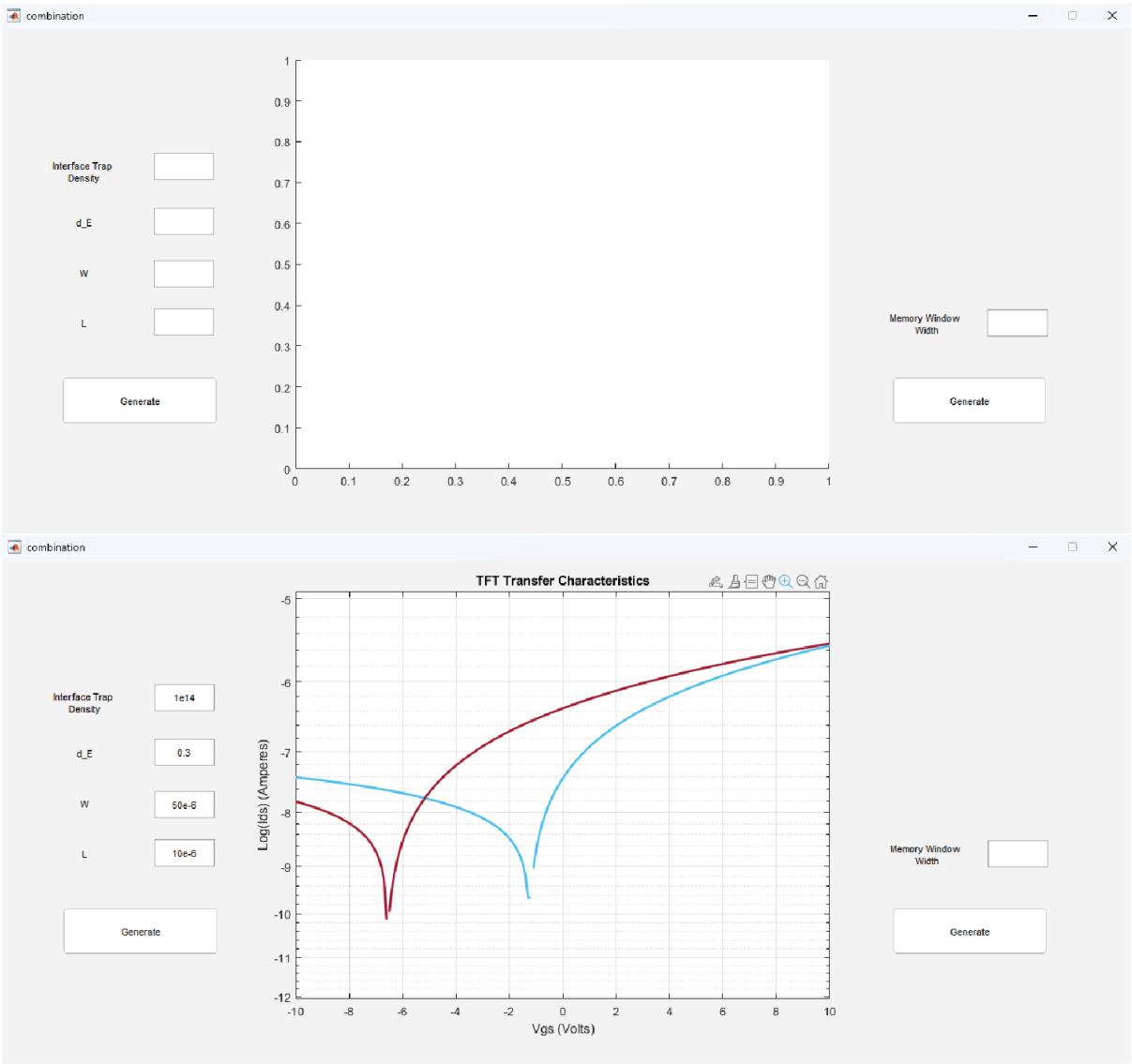


Figure 4.6: Mode-1 of GUI (Insert Interface Trap Density to retrieve visual representation of Resultant Memory Window)

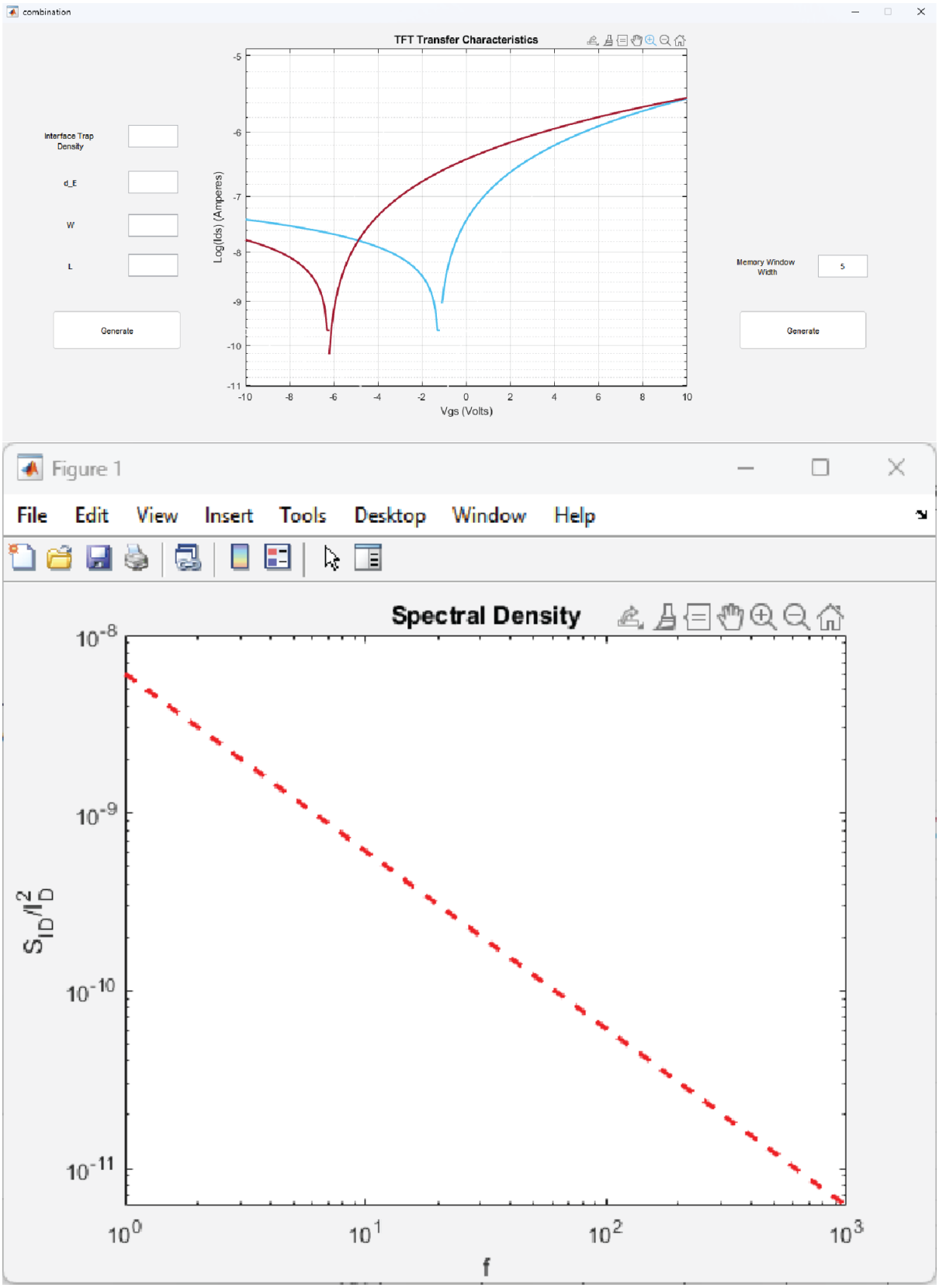


Figure 4.7: Mode-2 of GUI(Insert size of Memory Window to retrieve visual representation of the Memory Window alongside the Noise Profile

## 4.3 Limitations

### 4.3.1 Traditional Transfer Equations

- **Hysteresis Behavior**: Traditional TFT models are unable to capture the hysteresis behavior intrinsic to FeTFTs. Ferroelectric materials exhibit a polarization hysteresis loop, which significantly influences the device's electrical characteristics. Without including polarization effects, models cannot predict the bistable states necessary for non-volatile memory applications.
- **Threshold Voltage Shifts**: The lack of polarization modeling leads to inaccuracies in predicting threshold voltage shifts, which are critical for understanding the switching behavior and reliability of FeTFTs.

### 4.3.2 Larger Memory Window

- **Memory Window Prediction**: Accurate prediction of the memory window is essential for designing FeTFTs for memory applications. Traditional models fail to account for the dual stable states created by polarization, leading to unreliable memory window estimations.
- **Device Optimization**: Inaccurate memory window predictions hinder the ability to optimize FeTFTs for non-volatile memory, affecting data retention and endurance performance.

### 4.3.3 Transistor's Off Current

- **Leakage Current Estimation**: Traditional models do not accurately estimate the off-state leakage current in FeTFTs. The unique properties of ferroelectric materials, such as high trap densities, influence leakage currents, requiring specialized modeling approaches.
- **Operational Efficiency**: Inaccurate off current models lead to challenges in reducing leakage currents, which are crucial for enhancing the operational efficiency and power consumption of FeTFTs.

### 4.3.4 Drain Current Response

- **Dynamic Drain Current**: The ferroelectric layer's influence on drain current during reverse gate voltage sweeps is not captured by traditional models. This dynamic response complicates the extraction and accurate modeling of low-frequency noise, which is important for noise-sensitive applications.
- **Noise Modeling**: The premature response of drain current affects the accuracy of low-frequency noise models, making it difficult to predict and mitigate noise in FeTFTs.

### 4.3.5 Noise Integration

- **Noise Data Integration**: Traditional models lack mechanisms to integrate noise data specific to ferroelectric materials. Accurate noise modeling requires incorporating $1/f$ noise and other low-frequency noise characteristics unique to FeTFTs.

- **Model Fidelity**: Without precise noise integration, the models cannot accurately reflect the real-world performance of FeTFTs, affecting the reliability and design of noise-optimized devices.

### 4.3.6 Off Current Model Parameters

- **Parameter Refinement**: Existing parameters for modeling off current need refinement to account for the specific properties of ferroelectric materials. Factors such as increased trap density and complex carrier transport mechanisms must be included for accurate modeling .

- **Accurate Prediction**: Refined parameters are essential for accurately predicting off current, ensuring reliable characterization and performance optimization of FeTFTs.

### 4.3.7 Polarization Model

- **Polarization Switching**: A robust polarization model is required to simulate the time-dependent polarization switching behavior in FeTFTs accurately. This includes capturing the impact of polarization on the device's electrical characteristics.

- **Hysteresis Simulation**: Properly simulating hysteresis and memory effects is crucial for FeTFT applications, particularly in non-volatile memory, where data retention and switching behavior depend on accurate hysteresis modeling.

## 4.4 Future Improvements

### 4.4.1 Implementation of Polarization Model

- **Hysteresis Simulation**: Incorporating a detailed polarization model into FeTFT simulations will allow for accurate representation of the hysteresis loop characteristic of ferroelectric materials. This model will need to account for the non-linear and history-dependent nature of polarization switching.

- **Improved Predictive Accuracy**: By integrating polarization effects, the model will provide more accurate predictions of the device's behavior under different operating conditions, especially for applications requiring non-volatile memory.

### 4.4.2 Enhanced Noise Integration

- **Comprehensive Noise Modeling**: Enhanced noise integration involves identifying and modeling the various noise sources specific to ferroelectric materials, such as $1/f$ noise and thermal noise. This requires sophisticated techniques to accurately characterize and incorporate these noise sources into the device model.

- **Noise Data Utilization**: Using precise noise data in FeTFT models will improve their accuracy, leading to better noise predictions and more reliable device performance in noise-sensitive applications.

### 4.4.3 Optimized Off Current Model Parameters

- **Parameter Refinement**: Detailed analysis and adjustment of parameters that influence off current, such as trap densities and tunneling effects, will lead to more accurate off-state current predictions. This refinement process will improve the overall accuracy of the FeTFT models.
- **Model Precision**: Optimizing these parameters will enable more precise performance predictions, aiding in the design and evaluation of FeTFTs for various applications.

### 4.4.4 Optimization of Transistor's Off Current

- **Leakage Current Modeling**: Developing better strategies within the model to minimize off-state leakage current will lead to more accurate simulations. This includes modeling the effects of material properties and device structure on leakage.
- **Efficiency Predictions**: Accurate modeling of off current will improve predictions of the power efficiency and operational reliability of FeTFTs, particularly important for low-power applications.

### 4.4.5 Improvement in Drain Current Response

- **Dynamic Response Modeling**: Improving the model to capture the dynamic response of drain current, especially during transient conditions and reverse gate voltage sweeps, will enhance the accuracy of noise simulations.
- **Accurate Noise Characterization**: More precise modeling of drain current response will enable better characterization and prediction of low-frequency noise, leading to improved noise performance in FeTFTs.

### 4.4.6 Enhanced Memory Window Convergence

- **Memory Window Modeling**: Enhancing the model to better predict the memory window characteristics at peak gate voltages will ensure consistent simulation results. This includes accounting for factors such as polarization fatigue and retention loss.
- **Reliable Operation Predictions**: Improved convergence in memory window modeling will result in more reliable predictions of FeTFT performance in memory applications, ensuring consistent device operation over time.

### 4.4.7 Refinement of Hysteresis Modeling

- **Advanced Hysteresis Models**: Developing sophisticated models that accurately represent the complex hysteresis behavior in FeTFTs will involve both empirical and theoretical approaches. These models should simulate the impact of varying operational conditions on hysteresis accurately.
- **Predictive Capabilities**: Refined hysteresis modeling will improve the predictive accuracy of FeTFT simulations, leading to better understanding and optimization of device performance.

### 4.4.8 Modification of Transfer Characteristics Equation

- **Transfer Equation Enhancement**: Modifying the transfer characteristics equations to include terms that account for low-frequency noise behavior specific to FeTFTs will result in more accurate simulations. This includes incorporating noise from polarization switching and other ferroelectric effects.
- **Model Fidelity**: Improved transfer equations will increase the fidelity of FeTFT models, providing more accurate and reliable simulations of device behavior under real-world operating conditions.

We have already attempted the implementation of polarization model by applying the empirical model called the Hyperbolic Tangent Function. The result is staggering and provides insight to more areas to work on in the future.

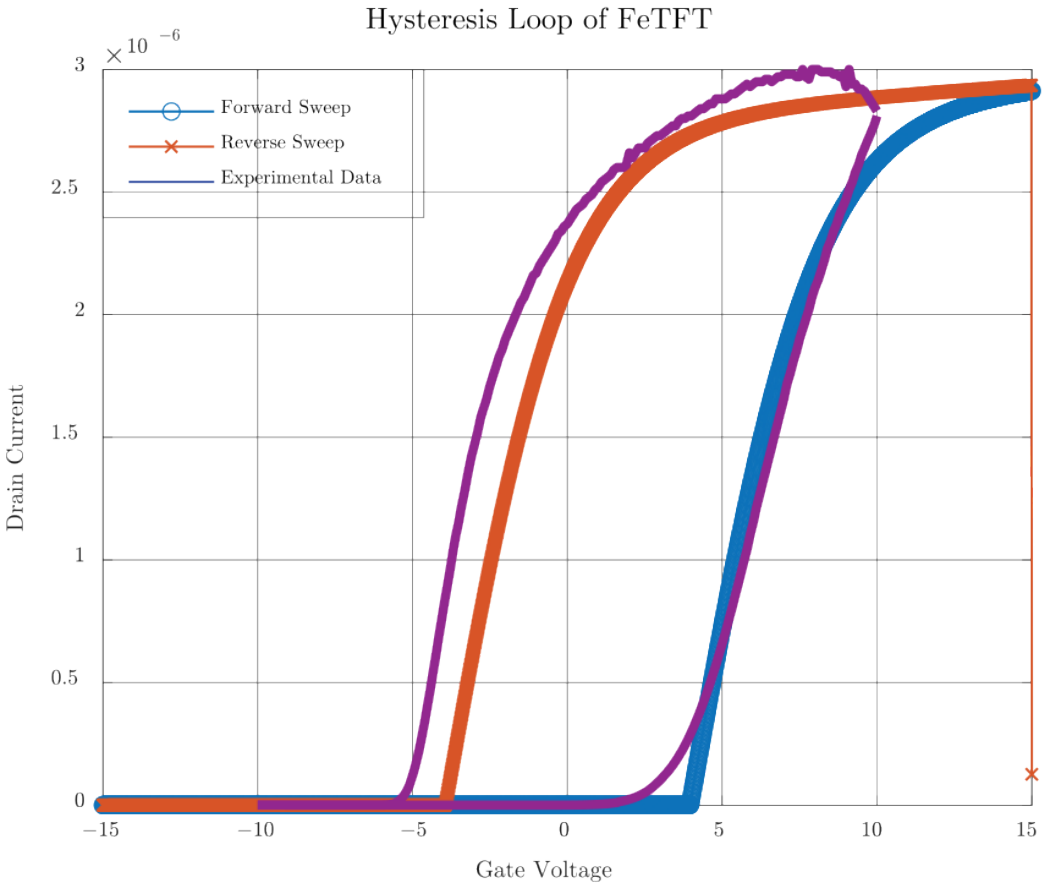


Figure 4.8: Implementation of Polarization model in Traditional TFT equations

# Chapter 5

# Demonstration of Outcome Based Education (OBE)

## 5.1 Course Outcomes (COs) Addressed

Table 5.1: COs addressed in EEE 4800 for Project and Thesis.

| COs | CO Statement | POs | Tick (✓) EEE 4800 |
|---|---|---|---|
| **CO1** | Identify a contemporary real life problem related to electrical and electronic engineering by reviewing and analyzing existing research works. | PO2 | ✓ |
| **CO2** | Determine functional requirements of the problem considering feasibility and efficiency through analysis and synthesis of information. | PO4 | ✓ |
| **CO3** | Select a suitable solution and determine its method considering professional ethics, codes and standards. | PO8 | ✓ |
| **CO4** | Adopt modern engineering resources and tools for the solution of the problem. | PO5 | ✓ |
| **CO5** | Prepare management plan and budgetary implications for the solution of the problem. | PO11 | ✓ |
| **CO6** | Analyze the impact of the proposed solution on health, safety, culture and society. | PO6 | ✓ |
| **CO7** | Analyze the impact of the proposed solution on environment and sustainability. | PO7 | ✓ |
| **CO8** | Develop a viable solution considering health, safety, cultural, societal and environmental aspects. | PO3 | ✓ |
| **CO9** | Work effectively as an individual and as a team member for the accomplishment of the solution. | PO9 | ✓ |
| **CO10** | Prepare various technical reports, design documentation, and deliver effective presentations for demonstration of the solution. | PO10 | ✓ |
| **CO11** | Recognize the need for continuing education and participation in professional societies and meetings. | PO12 | ✓ |

## 5.2 Aspects of Program Outcomes (POs) Addressed

Table 5.2: POs addressed in EEE 4800 for Project and Thesis

| POs | Statement | Different Aspects | Tick ( ✓ ) |
|---|---|---|---|
| **PO2** | **Problem analysis:** Identify, formulate, research literature and analyse complex electrical and electronic engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences. | | ✓ |
| **PO4** | **Investigation:** Conduct investigations of complex electrical and electronic engineering problems using research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions. | Design of experiments | ✓ |
| | | Analysis and interpretation of data | ✓ |
| | | Synthesis of information | ✓ |
| **PO6** | **The engineer and society:** Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to professional engineering practice and solutions to complex electrical and electronic engineering problems. | Societal | ✓ |
| | | Health | ✓ |
| | | Safety | ✓ |
| | | Legal | ✓ |
| | | Cultural | ✓ |
| **PO7** | **Environment and sustainability:** Understand and evaluate the sustainability and impact of professional engineering work in the solution of complex electrical and electronic engineering problems in societal and environmental contexts. | Societal | ✓ |
| | | Environmental | ✓ |
| **PO8** | **Ethics:** Apply ethical principles embedded with religious values, professional ethics and responsibilities, and norms of electrical and electronic engineering practice. | Religious values | ✓ |
| | | Professional ethics and responsibilities | ✓ |
| | | Norms | ✓ |
| PO9 | **Individual work and Teamwork:** Function effectively as an individual, and as a member or leader in diverse teams and in multi-disciplinary settings. | Diverse teams | ✓ |
| | | Multi-disciplinary settings | ✓ |

| POs | Statement | Different Aspects | Tick ( ✓ ) |
|---|---|---|---|
| PO10 | Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions. | Comprehend and write effective reports | ✓ |
| | | Design documentation | ✓ |
| | | Make effective presentations | ✓ |
| | | Give and receive clear instructions | ✓ |
| PO11 | Project management and finance: Demonstrate knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments. | Engineering management principles | ✓ |
| | | Economic decision-making | ✓ |
| | | Manage projects | ✓ |
| | | Multidisciplinary environments | ✓ |

Table 5.3: Justification of the COs and corresponding POs

| COs | POs | Explanation/Justification |
|---|---|---|
| CO1 | PO2 | Our thesis project directly aligns with CO1 by examining a contemporary issue in electrical and electronic engineering—specifically, the low-frequency noise characteristics of ferroelectric thin film materials—through an analysis of existing research, thus contributing to the advancement of knowledge in the field. |
| CO2 | PO4 | Our thesis project fits with CO2 as it figures out what's needed to study low-frequency noise in ferroelectric thin films. By looking closely at the information and combining it, it checks if the methods are practical and efficient, helping solve problems in electrical and electronic engineering. |
| CO3 | PO8 | Our thesis project aligns with CO3 by selecting appropriate methods to study low-frequency noise in ferroelectric thin film materials while adhering to professional ethics, industry standards, and codes of conduct. This ensures integrity and reliability in research practices within the field of electrical and electronic engineering. |
| CO4 | PO5 | Our thesis project aligns with CO4 by employing modern engineering resources and tools to investigate low-frequency noise in ferroelectric thin film materials. Utilizing advanced equipment and software enhances data collection, analysis, and interpretation, facilitating comprehensive research outcomes in electrical and electronic engineering. |

| | | |
|---|---|---|
| CO5 | PO11 | Our thesis project meets CO5 by devising a management plan and considering budgetary implications for studying low-frequency noise in ferroelectric thin film materials. This ensures efficient resource allocation and effective project management, essential for the successful implementation of the research endeavor in electrical and electronic engineering. |
| CO6 | PO6 | CO6 relates to our thesis by examining how the low-frequency noise model for FETFTs improves electronic device performance, leading to safer and more reliable technology. Mitigating noise impacts enhances the reliability of consumer electronics, influences cultural reliance on technology, and benefits society through better device functionality. |
| CO7 | PO7 | CO7 relates to our thesis by analyzing how the low-frequency noise model for FETFTs can lead to more efficient and reliable electronic devices, reducing energy consumption and extending device lifespan. This contributes to environmental sustainability by minimizing electronic waste and reducing the need for frequent replacements, thereby lowering the overall environmental footprint of electronic products. |
| CO8 | PO3 | Our thesis on low-frequency noise modeling of FETFTs addresses CO8 by enhancing device performance and reliability, ensuring safe and stable operation to prevent malfunctions. It also considers cultural and societal aspects by improving the technology people rely on and focuses on environmental sustainability by reducing energy consumption and electronic waste, contributing to efficient, longer-lasting devices. |
| CO9 | PO9 | Our thesis showcases our ability to conduct independent research while collaborating with our advisor and peers. Through regular meetings, presentations, and peer feedback sessions, we demonstrate effective teamwork skills essential for problem-solving and professional growth. This aligns with CO9 of the OBE framework, emphasizing both individual contribution and collaborative effort in achieving research objectives |
| CO10 | PO10 | Our thesis work involves preparing technical reports, design documentation, and presentations to communicate our findings effectively. Through these deliverables, we demonstrate proficiency in documenting research outcomes and conveying complex technical information to peers and faculty members. This aligns with CO10 of the OBE framework, emphasizing the importance of clear communication and presentation skills in engineering practice. |
| CO11 | PO12 | Our thesis on low-frequency noise modeling of FETFTs implements CO11 by emphasizing ongoing education and participation in professional societies. This includes staying updated with the latest research, incorporating new methodologies, joining societies like IEEE, attending conferences, and publishing findings to contribute to and stay informed about advancements in the field. |

## 5.3 Knowledge Profiles (K3 – K8) Addressed

Table 5.4: Knowledge Profiles (K3 – K8) addressed in EEE 4800 for Project and Thesis

| K | Knowledge Profile (Attribute) | Tick (✓ ) |
|---|---|---|
| **K3** | A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline | ✓ |
| **K4** | Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline | ✓ |
| **K5** | Knowledge that supports engineering design in a practice area | ✓ |
| **K6** | Knowledge of engineering practice (technology) in the practice areas in the engineering discipline | ✓ |
| **K7** | Comprehension of the role of engineering in society and identified issues in engineering practice in the discipline: ethics and the engineer's professional responsibility to public safety; the impacts of engineering activity; economic, social, cultural, environmental and sustainability | ✓ |
| **K8** | Engagement with selected knowledge in the research literature of the discipline | ✓ |

## 5.4 Attributes of Ranges of Complex Engineering Activities (A1 – A5) Addressed

Table 5.5: Attributes of Ranges of Complex Engineering Activities (A1 – A5)

| A | Range of Complex Engineering Activities | Tick (✓ ) |
|---|---|---|
| **Attribute** | Complex activities means (engineering) activities or projects that have some or all of the following characteristics: | ✓ |
| Range of resources | **A1:** Involve the use of diverse resources (and for this purpose resources include people, money, equipment, materials, information and technologies) | ✓ |
| Level of interaction | **A2:** Require resolution of significant problems arising from interactions between wide-ranging or conflicting technical, engineering or other issues | ✓ |
| Innovation | **A3:** Involve creative use of engineering principles and research-based knowledge in novel ways | ✓ |
| Consequences for society and the environment | **A4:**Have significant consequences in a range of contexts, characterized by difficulty of prediction and mitigation | ✓ |
| Familiarity | **A5:**Can extend beyond previous experiences by applying principles-based approaches | ✓ |

Table 5.6: Justification of Attributes addressed

| A | Explanation/Justification |
|---|---|
| **A1** | In our thesis, we utilize a wide range of resources, including literature reviews, laboratory equipment, research materials, and computational tools, to investigate the low-frequency noise characteristics of Ferroelectric Thin Film Transistors (FeTFTs). |
| **A2** | We encounter significant challenges stemming from interactions between technical and engineering issues, such as optimizing FeTFT memory cell structures for improved performance while minimizing noise interference and ensuring compatibility with existing memory architectures. |
| **A3** | Our research involves creatively applying engineering principles and research-based knowledge to explore innovative methods of controlling and mitigating low-frequency noise in FeTFT-based memory devices, contributing to advancements in memory technology. |
| **A4** | The outcomes of our thesis research have substantial consequences for society and the environment, as advancements in memory technology impact various contexts, including data storage, computing efficiency, and energy consumption, with implications for sustainability and societal well-being. |
| **A5** | Our thesis extends beyond previous experiences by applying principles-based approaches to address challenges in FeTFT memory design, pushing the boundaries of knowledge and expertise in electronic engineering. |

## 5.5 Use of Complex Engineering Problems

Our project delves into the transformative role of complex engineering problems in education. These challenges serve as catalysts for critical thinking, problem-solving, and interdisciplinary collaboration. By immersing students in real-world scenarios, we aim to cultivate resilient, resourceful engineers adept at tackling tomorrow's challenges with creativity and ethical discernment.

## 5.6 Socio-Cultural, Environmental, And Ethical Impact

### 5.6.1 Economical Viability

The economic success of our research hinges on the substantial potential benefits it could yield. If we successfully model low-frequency noise, we can revolutionize capacitorless DRAM design by incorporating this understanding. This could significantly reduce the physical space needed for memory and transition volatile memory into more stable non-volatile memory solutions.

Moreover, FeTFTs provide a significant economic advantage by seamlessly fitting into existing CMOS processes with minimal adjustments. This integration not only enhances the capabilities of CMOS-based devices but also ensures cost-effectiveness in advancing semiconductor technologies. These advancements highlight our research's potential to innovate memory technology, making electronic devices more efficient and dependable.

### 5.6.2 Environmental Impact

Our research places a strong emphasis on energy efficiency, aiming to develop innovations that minimize power consumption and contribute to the advancement of sustainable technologies. We prioritize a production process that is compatible across manufacturing, aiming to reduce costs and environmental impact while ensuring scalability and accessibility in the market.

Furthermore, we are actively engaged in ongoing research focused on addressing end-of-life considerations. Our goal is to extend the lifecycle of our technologies and minimize electronic waste, supporting environmental stewardship and aligning with global initiatives promoting sustainable practices.

In addition to sustainability efforts, we are dedicated to achieving high performance and durability in our technologies. By creating robust solutions, we aim to set new standards for reliability and longevity, meeting the needs of both consumer electronics and industrial applications. These initiatives demonstrate our commitment to advancing technology that is both environmentally responsible and capable of delivering exceptional performance in today's competitive marketplace.

### 5.6.3 Ethical Impact

Our research on low-frequency noise modeling in ferroelectric thin-film transistors (FeTFTs) encompasses significant ethical considerations that extend across multiple dimensions. The primary aim is to utilize Hooge's noise model to develop a noise profile for FeTFTs, crucial for enhancing device performance. Ethically, this research addresses public safety by improving device reliability and reducing the risk of malfunctions that could harm users. It also promotes environmental sustainability through the development of more efficient devices that consume less energy and produce less electronic waste. Furthermore, the project upholds ethical standards in engineering education by emphasizing integrity in research practices and meeting educational outcomes related to problem-solving and professional responsibility. In research, it maintains integrity by following rigorous methodologies, ensuring accuracy, transparency, and accountability in the dissemination and application of its findings for societal and environmental benefit.

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