Islamic University of Technology, Bangladesh

Analysis of Impact Mechanical Stress on Flexible Electronics: Conventional Design vs Split Channel Design

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DECLARATION

We, Farhan Abrar, Ferdaus Zamal Siddiqui and Tahmid Hasan Muttaky, declare that this thesis titled, *'Analysis of Impact Mechanical Stress on Flexible Electronics: Conventional Design vs Split Channel Design'* and the work presented in it is our own. We confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Any part of this thesis has not been submitted for any other degree or qualification at this University or any other institution.
- Where we have consulted the published work of others, this was always clearly attributed.

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Abstract

As semiconductor devices become ubiquitous in harsh environments, from wearable gadgets to environmental sensors, their vulnerability to mechanical impacts—like drops, debris, or accidental knocks—poses a critical reliability challenge. Unlike gradual stresses, these sudden impacts generate extreme localized forces that can permanently degrade device performance. This research investigates a novel split-channel MOSFET architecture as a solution to mitigate such impact-induced damage. Using a comprehensive simulation framework that couples mechanical impact analysis with electrical performance modeling, we compare conventional transistors against split-channel designs where the active region is divided into isolated parallel sub-channels.

The results demonstrate that the air gaps between sub-channels act as powerful mechanical barriers, confining stress to the immediate impact zone and preserving the functionality of unaffected channels. This design enables graceful performance degradation rather than catastrophic failure. Our analysis shows that split-channel architectures can reduce electrical performance degradation by up to 1.59 times compared to conventional designs under identical impact conditions. The core protection mechanism is traced to the massive acoustic impedance mismatch between silicon and air, which reflects over 99.9% of the stress wave energy at each gap.

While the approach introduces a trade-off in the form of a larger chip area or a reduced current density for a given footprint, it provides a compelling architectural strategy for applications where mechanical resilience is paramount. This work establishes the split-channel architecture as a viable path toward creating more robust and reliable electronics for real-world conditions, offering designers a new tool to enhance durability without relying solely on external packaging.

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List of Acronyms

CMOS: Complementary Metal-Oxide-Semiconductor
IF: Improvement Factor
IoT: Internet of Things
MEMS: Micro-Electro-Mechanical Systems
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS: N-type Metal-Oxide-Semiconductor
PMOS: P-type Metal-Oxide-Semiconductor
TFT: Thin-Film Transistor
g_m: Transconductance
I-D: Drain Current
V-DS: Drain-to-Source Voltage
V-GS: Gate-to-Source Voltage
V-TH: Threshold Voltage
W-eff: Effective Width

CHAPTER 1
INTRODUCTION

1.1 Background and Motivation

A scenario might happen when during manufacturing assembly, a technician drops a small screw from working height onto a circuit board. Or a fly might land on an exposed sensor or a raindrop can strike on a solar cell. These seem minor events, but in a nanoscale or microscale device, the impact can generate localized stress concentrations at several gigapascals levels at the point of contact, which is well beyond the yield strength of silicon.

They create sudden mechanical loading that differs fundamentally from the gradual, uniform stresses that devices experience from thermal expansion or substrate bending. These impact events share common characteristics: they occur suddenly, concentrate force in localized regions, and potentially cause irreversible material damage.

In modern times, semiconductor devices are used everywhere and in all forms of diverse and challenging environments. While integrated circuits generally remain protected within rigid packaging in controlled conditions, many applications require devices that withstand direct environmental exposure. During assembly and handling, accidental events may occur as well.

This is why understanding impact mechanical stress in depth is crucial for electronic devices. However, from a research perspective, impact mechanical stress remains understudied and poorly understood. The semiconductor industry lacks knowledge on both how these transient, high-magnitude forces degrade device performance and practical design strategies to overcome such damage.

This knowledge gap becomes increasingly critical as devices shrink and applications expand. Miniaturization reduces the energy required to cause damage, while deployment in uncontrolled environments increases exposure frequency.

A sensor node in an agricultural field may experience hundreds of impact events from windborne debris over its operational lifetime. A wearable device worn during sports activities encounters repeated mechanical shocks. Without understanding how these impacts affect electrical performance and without architectural solutions to enhance resilience, device reliability in real-world conditions remains uncertain.

Recent work in flexible electronics has explored split-channel transistor architectures, where a single continuous channel is divided into multiple parallel sub-channels separated by isolation gaps. Initial investigations demonstrated remarkable tolerance to bending

stress in display applications. However, the research scope has been limited mostly to display applications and bending forces so far.

Whether split-channel architecture can protect against localized impact damage in conventional CMOS devices is a question that has not been explored in depth yet. This research addresses that question through systematic modeling and simulation-based analysis and comparative investigation.

1.2 Research Problem

Several critical gaps limit our ability to design mechanically resilient semiconductor devices:

Insufficient understanding of impact stress mechanisms: While extensive literature is available on continuous mechanical stress effects on carrier mobility and threshold voltage, the specific mechanisms by which sudden, localized impacts degrade MOSFET electrical characteristics lack comprehensive characterization.

The transition from mechanical stress fields to electrical parameter changes involves complex coupling between fracture mechanics, lattice damage, and carrier transport that existing models cannot adequately capture.

Absence of architectural solutions for impact resilience: Current mitigation strategies such as stress liners, strain-engineered substrates, protective packaging etc. primarily address continuous stress or exploit strain for performance enhancement often with a trade-off in terms of miniaturization, flexibility, and cost. They offer minimal protection against localized impacts.

Split-channel architectures show promise but remain underexplored for impact stress in CMOS technologies.

Lack of predictive simulation frameworks. Existing tools analyze either mechanical stress distributions or electrical device characteristics, but not their integrated coupling under dynamic impact conditions. Engineers lack the ability to predict performance degradation from specified impact scenarios or to optimize device architectures for expected threat environments.

Missing design guidelines. Without quantitative understanding of how impact size, energy, and device geometry affect degradation, designers cannot make informed trade-offs between performance, area, and resilience. The semiconductor industry needs practical guidance on when architectural innovations like split channels provide meaningful benefits and when conventional designs are sufficient.

1.3 Research Objectives

The objectives of this research are following:

Develop an integrated simulation framework that couples mechanical impact dynamics with MOSFET electrical characteristics, allowing prediction of current-voltage degradation from specified impact conditions.

Quantitatively compare conventional and split-channel architectures under controlled impact scenarios representing realistic events to simulate impact stress from minor contact to severe collision.

Identify physical mechanisms behind the observed performance differences, particularly the role of isolation gaps as mechanical barriers and the spatial extent of damage in each architecture.

Provide performance metrics (degradation factors, improvement ratios, damage isolation effectiveness) that enable engineers to evaluate architecture selection for specific applications and threat environments.

1.4 Research Question

The research question can be shaped as: **How does impact mechanical stress affect the I-V characteristics of MOSFETs, and how do split-channel designs compare to conventional structures under such conditions?**

This question guides the investigation through two phases: first, understanding the fundamental physics of impact-induced electrical degradation; second, evaluating whether architectural segmentation provides meaningful protection and under what conditions such protection is effective.

1.5 Expected Contributions

This research is expected to contribute to the field of mechanically resilient semiconductor design in several ways.

Novel architectural approach for impact resilience. This work is a pioneer work in comprehensive analysis of split-channel MOSFET architectures specifically for impact mechanical stress context in CMOS devices, extending beyond the scopes of previous works.

Integrated simulation framework. The development of a coupled mechanical-electrical simulation methodology enables prediction of device performance degradation from specified impact conditions, filling a critical gap in existing modeling tools that tends to address only mechanical or electrical domains separately.

Quantitative design guidelines. By systematically varying impact parameters and device geometries, this research establishes when split-channel architectures provide meaningful advantages and when conventional designs are sufficient, enabling informed design decisions based on application requirements.

Physical mechanism identification. The work identifies and quantifies the role of acoustic impedance mismatch at silicon-air interfaces as a mechanical barrier, providing fundamental understanding of damage isolation mechanisms that can inform future architectural innovations.

1.6 Research Significance

The findings of this research have significant implications for multiple domains of semiconductor technology.

Wearable and portable electronics. As health monitors, fitness trackers, and smartwatches become ubiquitous, these devices face repeated mechanical shocks during normal use. Understanding and mitigating impact damage directly translates to improved device longevity and user experience. Split-channel architectures could enable more durable wearables without requiring bulky protective casings.

Environmental sensing systems. IoT sensor nodes deployed in agricultural fields, industrial facilities, and remote monitoring stations operate in uncontrolled environments where impact from debris, insects, weather events, and maintenance activities is routine rather than exceptional. Enhanced impact resilience reduces maintenance costs and improves data reliability in critical infrastructure monitoring applications.

Flexible and stretchable electronics. The emerging field of flexible electronics for conformable sensors, electronic skin, and biomedical implants requires devices that maintain functionality despite mechanical deformation and occasional impacts. This research provides design strategies applicable to these next-generation technologies.

Manufacturing and reliability. Even for conventional packaged devices, impact events during assembly, testing, and handling contribute to manufacturing yield loss and field failures. Understanding impact damage mechanisms can inform better handling procedures and packaging designs, reducing costs across the semiconductor supply chain.

Broader technological impact. As electronics continue to miniaturize and proliferate into diverse applications—from automotive sensors to space-deployed systems—mechanical reliability becomes increasingly critical. This research addresses a fundamental challenge in making semiconductor devices robust enough for real-world deployment in harsh or uncontrolled conditions.

The shift from protected laboratory environments to ubiquitous real-world deployment demands that we understand and address mechanical reliability as thoroughly as we have addressed electrical performance. This research represents a step toward that goal.

CHAPTER 2
LITERATURE REVIEW AND METHODOLOGY

2.1 MOSFET Fundamentals

2.1.1 Operating Principles

The MOSFET is a type of transistor that controls current flow between source and drain terminals of the device through voltage applied to a gate electrode. In PMOS devices, negative gate voltage attracts holes to the silicon-oxide interface, forming a conductive channel. The drain current depends on both gate voltage (V_{GS}) and drain-source voltage (V_{DS}), with the device operating in either linear or saturation regions depending on the relative magnitudes of these voltages.

In the linear region, drain current increases approximately linearly with V_{DS} as the channel behaves like a voltage-controlled resistor. As V_{DS} increases, the channel eventually pinches off at the drain end, and the device enters saturation where current becomes relatively independent of V_{DS}. This transition occurs when the drain voltage becomes sufficient to deplete the channel at the drain side. [1]

2.1.2 Key Performance Parameters

Threshold voltage (V_{TH}): represents the minimum gate voltage required to form a conductive channel. It depends on oxide thickness, substrate doping concentration, oxide-silicon interface charges, and work function differences between gate and substrate materials. Any process that creates interface traps or modifies charge distributions will shift the threshold voltage.

Carrier mobility (μ): quantifies how easily charge carriers move through the channel under an applied electric field. Several scattering mechanisms limit mobility, including phonons (lattice vibrations), ionized impurities, and surface roughness at the silicon-oxide interface. Mechanical stress affects mobility both directly through lattice strain and indirectly by creating crystal defects that introduce additional scattering centers.

Transconductance (g_m), the derivative of drain current with respect to gate voltage, indicates the device's signal amplification capability. Mobility degradation and threshold voltage shifts both reduce transconductance, which degrades circuit performance.

These parameters determine device and circuit performance. Understanding how mechanical stress affects each parameter is essential for predicting impact-induced degradation.

2.2 Mechanical Stress in Semiconductors

2.2.1 Continuous versus Impact Stress

Mechanical stress in semiconductors manifests in fundamentally different ways depending on the loading conditions.

Continuous mechanical stress arises from persistent forces applied over extended timescales. Sources include thermal expansion mismatch between materials (during temperature cycling or operation), packaging-induced strain from encapsulation materials, and substrate bending in devices on flexible substrates. This stress type produces relatively uniform distributions across device structures and typically remains within material elastic limits. The semiconductor industry has extensively characterized continuous stress effects and even exploits controlled strain to enhance carrier mobility—this is the basis of strain engineering in modern CMOS technologies. Work by Peng et al. (2020) exemplifies this mature understanding of continuous stress in flexible electronics applications. [2]

Impact mechanical stress results from sudden force application over microsecond timescales. A projectile striking a device surface—whether a dropped tool during assembly, windborne debris, an insect making contact, or a water droplet—creates localized stress concentrations that can exceed silicon's yield strength (approximately 7 GPa). The stress distribution is highly non-uniform, with peak values at the impact point and rapid decay with distance. Unlike continuous stress, impact events can cause irreversible material damage including crystal lattice dislocations, microscopic fractures, and permanent structural changes. Choi et al. (2008) characterized impact effects in drop-test reliability studies, but comprehensive understanding remains limited. [3]

The distinction matters because design strategies that are effective against continuous stress—maintaining operation within elastic limits, exploiting strain for performance gain—do not adequately address impact damage. New approaches are needed.

2.2.2 Stress Effects on Electrical Performance

Mechanical stress affects MOSFET characteristics through multiple physical mechanisms. Lattice strain modifies semiconductor band structure, changing effective carrier mass and mobility. Tensile strain along the channel typically enhances electron mobility in NMOS devices, which is why strain engineering improves performance. However, compressive strain or non-uniform stress distributions can degrade mobility.

More significantly for impact stress, mechanical damage creates crystal defects—dislocations, vacancies, and broken bonds—that act as scattering centers for charge carriers and trap sites for charges. These defects reduce carrier mobility beyond simple strain effects and introduce interface states that shift threshold voltage. Lee et al. (2022) demonstrated that localized stress near the source region in 40-nm MOSFETs alters both V_{TH} and mobility by up to ±20%, significantly affecting circuit timing and power consumption. [4]

When stress exceeds material limits, plastic deformation and fracture introduce permanent structural changes. The affected regions exhibit severely degraded electrical properties including reduced mobility from extensive lattice disruption and large threshold shifts from high trap densities. For devices with single continuous channels, damage anywhere along the channel compromises the entire current path.

2.2.3 Current Mitigation Approaches

The semiconductor industry employs several strategies to manage mechanical stress, though none adequately address impact resilience.

Stress liners—thin silicon nitride films deposited over transistors—induce controlled compressive or tensile stress to enhance performance. However, these engineered stress films neither protect against impact nor prevent stress concentration from external loading, and may even amplify localized stress at impact sites.

Strain-engineered substrates, such as silicon-germanium source/drain regions or strained silicon-on-insulator structures, enhance performance through beneficial strain but offer no protection against sudden impacts.

Protective encapsulation with polymer or ceramic layers provides some physical shielding but conflicts with miniaturization goals, adds cost and complexity, and is impractical for applications requiring direct environmental exposure (sensors, MEMS devices).

These approaches primarily address continuous stress or exploit strain engineering, leaving impact mechanical stress—particularly for exposed devices in harsh environments—inadequately addressed.

2.3 Split-Channel Architecture

2.3.1 Concept and Prior Research

Split-channel architecture divides the channel region into multiple parallel sub-channels separated by insulating gaps rather than maintaining a single continuous conductive path. Each sub-channel operates independently, conducting current from source to drain through its own isolated silicon strip.

Urmi et al. (2022) pioneered this approach in flexible display technology, demonstrating polycrystalline silicon TFTs with split active layers (5×4 μm sub-channels). Their devices exhibited remarkable resilience to bending stress: no threshold voltage shift or on-current degradation occurred even at 1 mm bending radius—conditions that would destroy conventional TFTs. The isolation gaps prevented stress propagation across the device width, confining damage to directly stressed regions. [5]

However, this prior work focused narrowly on display applications with relatively large device dimensions, polycrystalline rather than single-crystal silicon, and continuous

bending rather than impact stress. Whether split-channel benefits extend to nanoscale CMOS under impact loading remained unexplored—a significant gap given the different physics involved.

2.3.2 Potential Advantages for Impact Resilience

Split-channel architecture offers several theoretical advantages against impact stress.

Spatial damage isolation: Impact damage affects only sub-channels in direct contact with the projectile, while physically separated channels may remain completely undamaged, maintaining their original electrical properties.

Mechanical decoupling: Gaps interrupt stress propagation paths. Stress waves traveling through silicon encounter air or oxide gaps with vastly different acoustic impedance, causing wave reflection and energy dissipation. This impedance mismatch creates mechanical barriers that attenuate stress transmission to distant channels.

Graceful degradation: Performance decreases proportionally with the number of damaged splits rather than catastrophically. If one of five channels fails, the device retains 80% of its original current capacity—enabling continued operation at reduced but functional performance.

Redundancy: Circuit designers can potentially exploit split redundancy, dynamically reconfiguring around failed channels or implementing fault-tolerant architectures that would be impossible with monolithic channels.

2.3.3 Design Trade-offs

Split-channel architecture introduces inherent compromises.

Area penalty: Isolation gaps consume space that would otherwise conduct current. A device with five 560 nm-wide channels separated by 300 nm gaps has approximately 12.5% less active silicon than a 3.2 μm continuous channel in the same footprint.

Fabrication complexity: Defining multiple narrow channels with precise gap dimensions requires advanced lithography and etching. Contact and routing become more complex with parallel current paths.

Uncertainty about benefit magnitude: Without quantitative analysis, designers cannot determine whether the resilience improvement justifies the area and complexity penalties. This uncertainty has limited split-channel adoption beyond niche applications.

2.4 Physics Models for Impact Analysis

To accurately simulate coupled mechanical-electrical behavior under impact stress, several established physics models are employed in the simulation framework.

2.4.1 Hertzian Contact Theory

Hertzian contact theory, developed by Heinrich Hertz in 1882, provides analytical solutions for stress and deformation when elastic bodies come into contact under load. The theory determines contact area size, pressure distribution, and subsurface stress fields based on material properties, geometry, and applied force. It remains the standard approach for analyzing elastic impact and indentation problems in materials science. [6]

2.4.2 Von Mises Yield Criterion

The von Mises criterion predicts material yielding under complex multiaxial stress states by combining all stress components into a single equivalent scalar. Material yields when this equivalent stress exceeds the uniaxial yield strength. Originally developed for ductile metals, the criterion has been successfully applied to silicon and semiconductor materials in fracture mechanics studies, providing a convenient damage assessment parameter across spatially varying stress fields. [7]

2.4.3 Acoustic Impedance and Wave Reflection

When stress waves encounter interfaces between materials with different acoustic impedances, partial reflection and transmission occur. Acoustic impedance characterizes a material's resistance to stress wave propagation. Silicon and air have dramatically different impedances, resulting in nearly complete stress wave reflection at silicon-air interfaces. This impedance mismatch forms the physical basis for stress isolation in split-channel architectures, where air gaps act as acoustic barriers. [8]

2.4.4 Model Integration

These established physics models integrate within the simulation framework: Hertzian contact theory determines the initial stress distribution from impact conditions, von Mises stress identifies damaged regions, and acoustic impedance mismatch quantifies stress attenuation across gaps. Coupling these mechanical models with MOSFET electrical characteristics enables comprehensive performance prediction under specified impact conditions.

2.5 Research Gap and Contributions

The literature review reveals critical gaps: while split-channel architectures demonstrate promise under continuous bending stress in specific applications, their behavior under localized impact stress in CMOS devices remains uninvestigated. Furthermore, no comprehensive modeling framework exists that couples impact mechanics, fracture behavior, acoustic wave propagation, and electrical degradation to predict performance changes from specified impact conditions.

This research addresses these gaps through systematic simulation-based analysis, quantitative comparison of conventional and split-channel designs, identification of

physical protection mechanisms, and establishment of design guidelines for architecture selection based on expected mechanical threat environments.

2.6 Research Methodology

This research employs a systematic simulation-based approach to investigate impact mechanical stress effects on MOSFET performance and compare conventional versus split-channel architectures. The methodology integrates mechanical stress analysis, fracture modeling, and electrical performance prediction through a multi-stage workflow.

2.6.1 Overall Research Framework

The complete investigation follows a structured progression:

1. **Device design and baseline characterization** using COMSOL Multiphysics
2. **Impact stress simulation** to determine mechanical stress distributions
3. **Mathematical modeling** to link mechanical damage with electrical degradation
4. **Performance comparison** between conventional and split-channel architectures
5. **Parametric analysis** across multiple impact scenarios

This framework enables controlled investigation of how device architecture influences resilience to impact stress while maintaining physics-based accuracy throughout the analysis chain.

2.6.2 COMSOL Multiphysics Simulation

Device Structure Design:

Two MOSFET architectures were designed and modeled in COMSOL Multiphysics:

- **Conventional MOSFET**: Single continuous channel with width W = 3.2 μm, length L = 2.0 μm, and device height h = 1.0 μm
- **Split-channel MOSFET**: Five parallel sub-channels (each 560 nm wide) separated by 300 nm air gaps, with the same overall dimensions

Both designs use identical gate oxide thickness (5 nm), source/drain dimensions, and doping profiles to ensure fair comparison. The PMOS structure was selected for analysis with appropriate substrate and well doping concentrations.

Carrier Distribution Analysis:

Before applying impact stress, carrier distribution (hole and electron concentrations) was simulated under normal bias conditions to verify proper device operation. This baseline characterization confirms that:

- Channel formation occurs correctly in both architectures
- Split-channel gaps provide electrical isolation without compromising functionality
- Current flow paths are properly established in each sub-channel

This validation step ensures that observed performance differences after impact stem from mechanical damage rather than flawed device design.

Impact Stress Simulation:

Mechanical impact was simulated by modeling tungsten sphere drops onto the MOSFET surface. The simulation workflow includes:

1. **Ball drop definition**: Spheres of varying radii (R = 10, 20, 50 μm) dropped from specified heights (H = 30, 60, 90 μm)
2. **Contact mechanics**: Dynamic contact between tungsten ball and silicon surface using COMSOL's contact pairs and penalty method
3. **Stress field calculation**: Von Mises stress distribution computed throughout the device structure during and immediately after impact
4. **Temporal analysis**: Transient simulation captures peak stress conditions

The simulation outputs provide detailed spatial stress distributions showing how mechanical energy propagates through conventional versus split-channel structures. Key observations include:

- In conventional MOSFETs, stress propagates uniformly across the entire channel width
- In split-channel MOSFETs, air gaps interrupt stress transmission, confining high stress to the directly impacted region

These stress field data serve as input to the subsequent mathematical modeling stage.

2.6.3 Mathematical Modeling Framework

The mathematical model translates mechanical stress distributions from COMSOL into electrical performance predictions through several integrated components.

Fracture Analysis and Damage Assessment:

Using stress field data from COMSOL, the mathematical model identifies damaged regions based on material strength criteria. The analysis incorporates:

- Multi-zone damage classification based on local stress magnitude
- Spatial damage extent calculation across the channel width
- For split-channel devices: per-split damage assessment accounting for acoustic impedance barriers at air gaps

This fracture analysis determines which portions of the device experience severe, moderate, light, or no damage.

Mobility Degradation Modeling:

Mechanical damage creates crystal defects that degrade carrier mobility. The model relates local stress levels to mobility reduction through empirically-calibrated degradation

functions. For split-channel devices, each sub-channel's mobility is evaluated independently based on the stress it experiences.

Spatial averaging across the damaged channel width yields effective device-level mobility that feeds into current-voltage calculations.

Threshold Voltage Shift Calculation:

Impact-induced lattice damage creates interface traps that shift threshold voltage. The model computes threshold shifts based on damage severity, with spatial integration across the channel providing device-level V_TH changes.

I-V Characteristic Generation:

Using the degraded mobility and shifted threshold voltage, the model generates complete current-voltage characteristics:

- **Output curves (I_D vs V_{DS})**: Showing drain current as a function of drain voltage for multiple gate voltages
- **Transfer curves (I_D vs V_{GS})**: Showing drain current as a function of gate voltage at fixed drain voltage

A smooth transition function ensures physically realistic curves without discontinuities between linear and saturation regions. Comparison of pristine versus post-impact I-V curves quantifies performance degradation.

2.6.4 Equal Effective Width Configuration

To enable fair comparison between architectures, an additional split-channel configuration was designed and analyzed:

- **Split-channel (equal width)**: Five 760 nm-wide sub-channels with 300 nm gaps, total device width W_total = 4.4 μm
- Effective channel width (3.8 μm) approximately matches conventional design (3.2 μm)

This configuration isolates the protective benefits of channel segmentation from inherent current advantages of wider devices. The same impact scenarios and mathematical modeling workflow were applied to this equal-width design.

2.6.5 Comparative Performance Analysis

For each impact scenario (9 total combinations of ball radius and drop height), the following metrics were extracted and compared:

Primary metrics:

- Original performance (pristine device current)
- Performance degradation percentage after impact
- Contact radius and maximum pressure at impact site

- Number of splits affected (split-channel only)

Comparative metrics:

- Improvement factor: ratio indicating how much better split-channel retains performance
- Damage isolation effectiveness: percentage of undamaged splits

Results were systematically organized to identify trends with impact size, energy, and device architecture.

2.6.6 Validation and Consistency Checks

Throughout the methodology, multiple validation steps ensure physical accuracy:

- Material properties verified against semiconductor literature
- Hertzian contact predictions compared with COMSOL stress distributions
- I-V curves checked for proper saturation behavior and physical limits
- Energy conservation verified in impact simulations
- Parametric trends examined for physical consistency

While experimental validation was not feasible within project scope, the physics-based modeling approach and systematic validation checks provide confidence in the theoretical predictions.

2.7 Expected Outcome

Based on the literature review, physics foundations, and research methodology, the following outcomes are anticipated from the comparative analysis of conventional and split-channel MOSFET architectures under impact mechanical stress:

2.7.1 Stress Propagation Behavior

- **Conventional MOSFET:** Stress propagates uniformly across the entire channel width, causing widespread degradation.
- **Split-Channel MOSFET:** Air gaps confine stress to directly impacted splits. Acoustic impedance mismatch (~50,000:1 between silicon and air) prevents stress transmission to adjacent splits, preserving their functionality.

2.7.2 Electrical Performance Degradation

- **Conventional MOSFET:** Significant current reduction expected as stress affects all current paths simultaneously.
- **Split-Channel MOSFET:** Reduced degradation expected as only damaged splits experience performance loss. Undamaged splits maintain original functionality and contribute full current, enabling graceful degradation.

2.7.3 Impact Scenario Dependence

- **Small, Localized Impacts:** Split-channel architecture expected to provide maximum protection. Improvement factor (IF) expected to be significant.
- **Medium Impacts:** Protection benefits expected to diminish as impact affects multiple splits.
- **Large, Distributed Impacts:** Split-channel advantage expected to be minimal as all splits experience damage. However, graceful degradation should still enable partial functionality.

2.7.4 Design Trade-offs

- **Active Area Penalty:** For constant outer device width, gaps reduce effective channel width by approximately 37.5%.
- **Equal-Width Configuration:** Split-channel devices with equivalent drive current require larger outer dimensions (4.4 μm versus 3.2 μm).

2.7.5 Expected Metrics

- **Degradation:** Conventional MOSFETs expected to show significant current reduction; split-channel devices expected to show less degradation under localized impacts.
- **Improvement Factor:** IF = (Degradation_conventional) / (Degradation_split-channel) expected to exceed unity, with higher values for localized impacts and lower values for distributed impacts.
- **Damage Confinement:** Split-channel devices expected to maintain undamaged sub-channels with pristine electrical characteristics.

CHAPTER 3
COMSOL MODELING AND SIMULATION

3.1 Introduction

This chapter presents the COMSOL Multiphysics simulation framework used to analyze mechanical stress distribution in MOSFET devices under impact loading. The simulation integrates two physics modules: semiconductor device physics for electrical characterization and multibody dynamics for mechanical impact analysis. This coupled approach enables examination of stress propagation patterns in conventional and split-channel architectures.

3.2 Device Structure Design

3.2.1 Conventional MOSFET Geometry

The conventional MOSFET was designed with the following specifications:

- Channel Length (L): 2.0 μm
- Channel Width (W): 3.2 μm
- Device Height (h): 1.0 μm
- Device type: PMOS

The geometry represents a single continuous channel region between source and drain terminals. The three-dimensional structure was modeled to capture realistic stress distribution during impact events.

3.2.2 Split-Channel MOSFET Geometry

The split-channel architecture divides the channel into isolated segments:

- Number of Splits: 5
- Individual Split Width: 400 nm
- Gap Width: 300 nm (air-filled)
- Total Active Width: 2.8 μm
- Overall dimensions matching conventional design

The air gaps provide both electrical isolation between splits and mechanical barriers to stress wave propagation. Each split functions as an independent current path from source to drain.

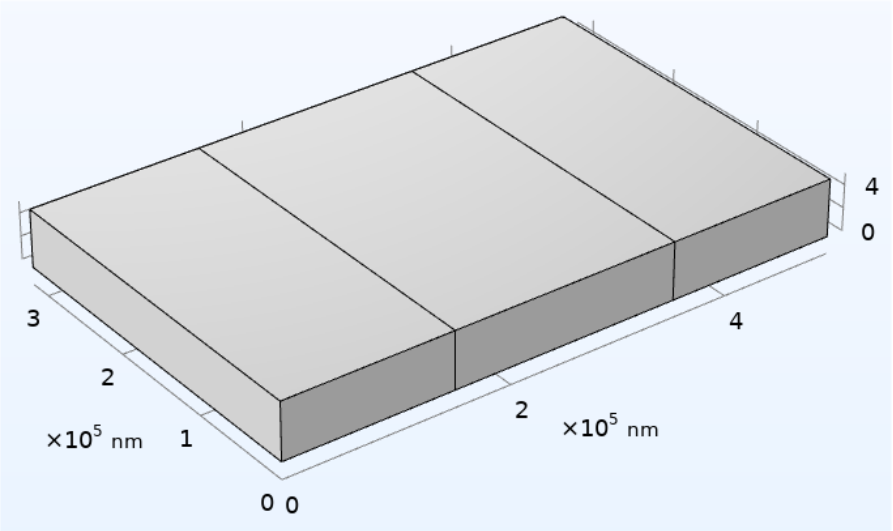


Fig. 3.1 Conventional MOSFET (Scaled)

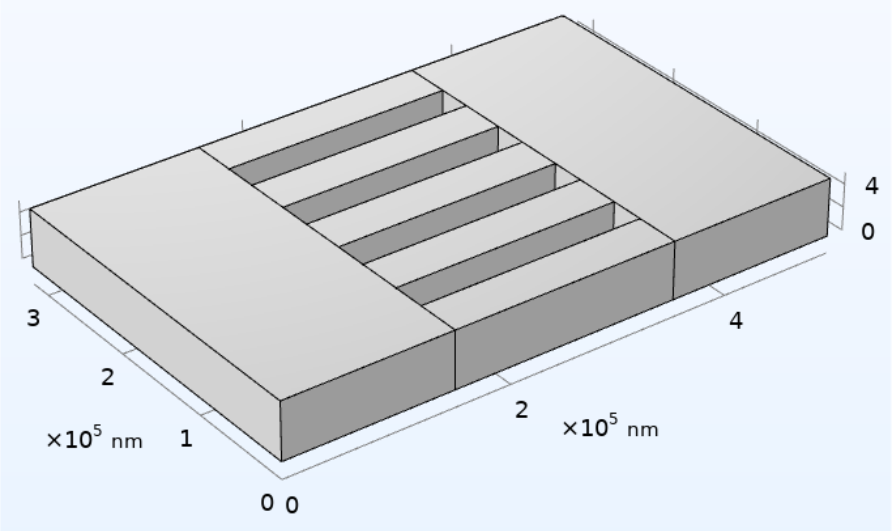


Fig. 3.2 Split Channel MOSFET (Scaled)

3.3 Physics Module Configuration

3.3.1 Semiconductor Physics

The Semiconductor module simulates PMOS device operation with appropriate material properties and doping profiles:

Material Properties:

- Silicon substrate with characteristic doping concentrations
- Heavily doped source and drain regions
- Lightly doped channel region
- Thin gate oxide layer

Physical Models:

- Drift-diffusion carrier transport
- Carrier recombination mechanisms
- Appropriate statistical distributions for carrier concentrations
- Analytic doping models for device regions

Boundary Conditions:

- Metal contacts at source, drain, and gate terminals
- Insulator interfaces at oxide-silicon boundaries
- Appropriate electrical isolation and continuity conditions

The model structure includes multiple gate regions corresponding to the splits in the split-channel design, each functioning independently.

3.3.2 Multibody Dynamics

The Multibody Dynamics module simulates the mechanical impact event using tungsten ball drops:

Impact Projectile:

- Tungsten (W) sphere used to represent rigid impact scenarios
- Tungsten selected for its high density and rigidity, representing worst-case impact conditions

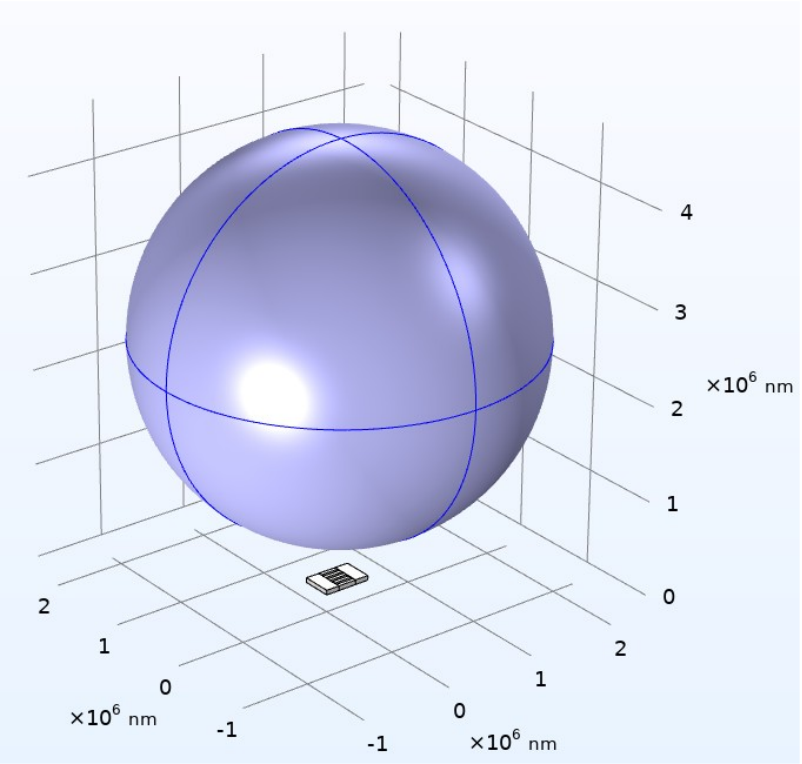


Fig. 3.3 Tungsten ball to simulate impact stress

Material Definition:

- Silicon with appropriate elastic properties
- Tungsten ball with characteristic high density and elastic modulus
- Linear elastic material behavior for both materials

Impact Configuration:

- Tungsten sphere positioned above device surface at specified height
- Gravitational loading to simulate free-fall drop event
- Contact interaction between ball and silicon surface
- Appropriate boundary constraints on device structure

Dynamic Analysis:

- Transient simulation capturing impact dynamics
- Time-dependent response with appropriate time resolution
- Simulation duration sufficient to capture peak stress conditions

3.4 Simulation Workflow

3.4.1 Study 1: Semiconductor Equilibrium

The first study establishes steady-state electrical operation before impact:

Objective: Determine carrier distribution and electric potential under operational bias conditions

Configuration: Stationary analysis of semiconductor physics with device biased in the on-state

Results Extracted:

- Hole concentration distribution
- Electron concentration distribution
- Electric potential field
- Verification of proper channel formation

This study confirms device functionality before applying mechanical stress.

3.4.2 Study 2: Impact Dynamics

The second study simulates the mechanical impact event:

Objective: Determine spatial stress distribution during impact

Configuration: Time-dependent analysis of multibody dynamics with ball drop simulation

Results Extracted:

- Von Mises stress field throughout device volume

- Surface displacement patterns
- Contact pressure distribution
- Temporal evolution of stress during impact

The simulation captures the complete impact event from initial contact through peak stress conditions.

3.5 Meshing Strategy

Appropriate mesh configuration ensures accurate stress field resolution:

- Refined mesh in channel region and anticipated impact area
- Coarser mesh in bulk regions for computational efficiency
- Free tetrahedral mesh elements
- Refinement at material interfaces and geometric features

Mesh density represents a balance between computational resource limitations and required solution accuracy.

3.6 Carrier Distribution Analysis

3.6.1 Conventional MOSFET

Carrier distribution results confirm proper PMOS operation:

Hole concentration: High concentration in the channel region beneath the gate when biased in the on-state, with accumulation at the silicon-oxide interface. Source and drain regions show elevated concentrations consistent with heavy doping.

Electron concentration: Low in the channel region as expected for PMOS operation. Higher concentration in the substrate body providing proper electrical isolation.

The visualization shows distinct source, drain, and channel regions with appropriate carrier distributions for device operation.

3.6.2 Split-Channel MOSFET

The split-channel design exhibits similar carrier behavior with architectural differences:

Channel formation: Each of the five splits independently forms a conductive channel when appropriately biased. The visualization clearly shows five parallel carrier accumulation regions separated by air gaps.

Electrical isolation: Zero carrier concentration in the gap regions confirms complete electrical isolation between splits. Each split operates as an independent device sharing common terminals.

Functionality verification: Well-defined channels in each split validate that architectural segmentation does not compromise basic device operation.

3.7 Impact Stress Distribution

3.7.1 Conventional MOSFET Response

When the tungsten ball impacts the conventional MOSFET surface, stress propagates uniformly across the device:

Surface deformation: Impact creates localized surface displacement at the contact point, with magnitude depending on impact conditions.

Stress propagation: Peak stress occurs at the impact center and decays radially outward. Stress extends continuously across the full channel width with no barriers to propagation. The entire channel region experiences elevated stress levels, though magnitude varies with position.

Subsurface effects: Stress penetrates through the device height, affecting the channel region where carrier transport occurs.

3.7.2 Split-Channel MOSFET Response

The split-channel architecture exhibits fundamentally different stress behavior:

Stress confinement: Impact stress concentrates in the directly impacted region. The visualization clearly shows localized high stress in one or a few splits, while distant splits experience minimal stress.

Gap barrier effect: Air gaps interrupt stress wave propagation. The material discontinuity creates acoustic impedance mismatch, causing stress reflection and preventing transmission to non-adjacent splits.

Spatial isolation: Depending on impact size, only a subset of splits experiences significant stress. Stress magnitude attenuates across gaps due to the barrier effect.

3.7.3 Comparative Visualization

The pressure distribution comparison highlights the architectural difference:

Conventional device: Stress distribution is continuous and relatively symmetric across the channel width, with smooth gradients from impact center outward.

Split-channel device: Stress distribution is discontinuous, with distinct high-stress regions separated by low-stress gaps. The visualization shows alternating stressed and unstressed regions corresponding to silicon splits and air gaps.

This spatial confinement forms the physical basis for improved resilience of split-channel designs, as undamaged splits can maintain functionality while damaged regions are isolated.

3.8 Model Validation

Several checks validate the simulation approach:

Physical consistency: Carrier distributions match theoretical expectations for PMOS devices with the design specifications.

Stress plausibility: Peak stress values align with expected magnitudes for the simulated impact conditions based on contact mechanics principles.

Energy behavior: Kinetic energy converts appropriately to elastic strain energy without unphysical losses or gains.

Qualitative verification: Stress patterns exhibit expected spatial characteristics and decay behavior.

3.9 Data Export for Mathematical Modeling

The COMSOL simulation provides stress field data that feeds into the mathematical analysis:

Exported information includes:

- Spatial stress distribution at relevant time points
- Contact characteristics and pressure patterns
- Stress values across the channel width for damage assessment

This coupling enables integration of mechanical simulation results with electrical performance prediction through mathematical modeling, as detailed in the following chapter.

CHAPTER 4
ELECTRICAL PERFORMANCE ANALYSIS

4.1 Mathematical modeling

To further analyze and compare electrical performance before and after impact, a mathematical model is incorporated based on findings from COMSOL simulation. The mathematical modeling follows actual material properties and is driven by realistic physics behavior.

4.1.1 Workflow

The electrical performance analysis requires to determine the stress distribution and resulting mechanical damage first, followed by determining electrical degradation and I-V curve characterization.

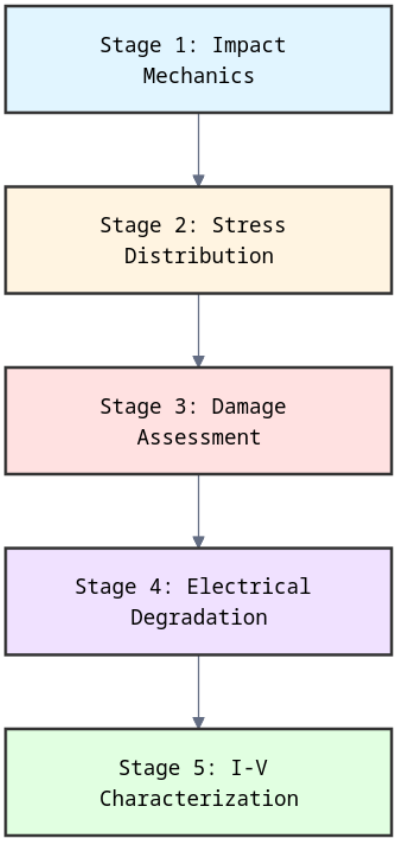


Fig 4.1 Mathematical Modeling Workflow

4.1.2 Material properties implementation

To ensure physical accuracy, the simulation incorporates experimentally-verified physical and electrical material properties for all components (silicon, tungsten and air) involved in the impact event and subsequent electrical behavior. Detailed properties are shown in Appendix A.

Incorporating these properties allows to model the impact event accurate to real-life. The high contrast between silicon and air acoustic impedances (ratio ~50,000:1) provides the physical basis for split-channel isolation effectiveness.

4.1.3 Determining contact area and impact force

To effectively consider impact of contact as the Tungsten ball drops on the MOSFET from a height H, the contact area needs to be determined. Impact velocity can be determined by,

$$v_{impact} = \sqrt{2gH}$$

Weight of the Tungsten ball along with impact velocity establishes the kinetic energy available for conversion into elastic strain energy and potential material damage. Resulting force can be determined by,

$$F_{impact} = m_w g \times \left(1 + \frac{v_{char}}{v_{impact}}\right)$$

where, v_{char} is the characteristic velocity of the contact system, shown in appendix A. The effective elastic modulus combines properties of both materials.

$$E_{eff} = \left[\frac{1-\nu_{Si}^2}{E_{Si}} + \frac{1-\nu_W^2}{E_W}\right]^{-1}$$

For elastic spheres in contact, the contact radius is given by:

$$a_{contact} = \sqrt[3]{\frac{3F_{impact}R}{4E_{eff}}}$$

The maximum contact pressure at the center of impact follows a hemispherical distribution:

$$p_{max} = \frac{3F_{max}}{2\pi a_{contact}^2}$$

4.1.4 Stress Propagation

The stress field extends both radially and vertically, with magnitude decreasing as a function of distance from the impact center. Using elastic half-space theory, the von Mises equivalent stress at any point (r, z) beneath the contact is modeled as:

$$\sigma_{vm}(r,z) = p_{max} \cdot \left(\frac{a_{contact}}{R_{total}} \right)^2 \cdot e^{\alpha R_{total}}$$

where, $R_{total}=\sqrt{(r^2+z^2)}$

The stress field is computed on a fine spatial grid spanning the device geometry, providing complete three-dimensional stress distribution for damage assessment.

4.1.5 Progressive Damage Identification

To account for material damage, a physics-based damage model is implemented that considers that damage severity in different distance taking acoustic impedances into account. High-stress regions show severe mobility reduction and substantial threshold voltage shifts, where low-stress regions experience minor degradation to electrical characteristics. Silicon's yield strength (σ = 7 GPa) serves as the reference for damage severity.

The mobility degradation follows the following relation within a region:

$$\mu_{degraded}(\sigma_{vm}) = \mu_0 \cdot f_{damage}(\sigma_{vm})$$

Where σ_{vm} accounts for damage severity in that region.

4.1.6 Split-Channel - Acoustic Barrier Effect:

For split-channel architectures, air gaps between splits introduce a physical barrier to stress propagation. When a stress wave traveling through silicon encounters an air gap, the dramatic difference in acoustic impedance causes nearly complete reflection of the mechanical wave.

The acoustic impedance of silicon differs drastically from air, resulting in a near-perfect reflection. Approximately 99.9% of the stress wave reflects at each silicon-air interface, dramatically attenuating stress transmission across gaps.

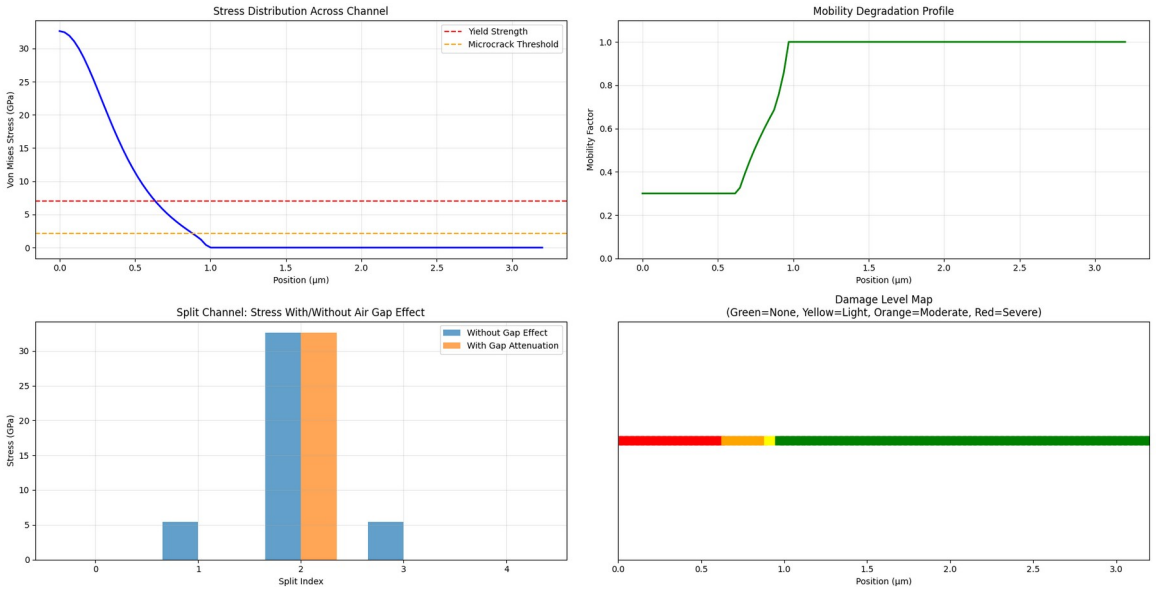


Fig. 4.2 Fracture analysis (Tungsten ball radius = 20 μm, drop height = 120 μm)

4.1.7 Electrical parameter degradation mapping

The spatially-varying damage profile translates directly to electrical parameter degradation through well-established carrier transport physics.

Mobility degradation and threshold voltage shift:

For the channel region spanning width W, the effective mobility becomes:

$$\mu_{eff} = \frac{1}{W}\int_0^W \mu_{degraded}(r)\,dr$$

The threshold voltage shift is calculated from trapped charge density induced by lattice damage:

$$\Delta V_{TH} = \frac{1}{W}\int_0^W \Delta V_{TH}(r)\cdot f_{damage}(r)\,dr$$

Overall Current Degradation:

The drain current in both linear and saturation regions scales with mobility and is affected by threshold shifts. The overall performance degradation factor can be determined:

$$\eta = \frac{I_{D,damaged}}{I_{D,pristine}} = \frac{\mu_{eff}}{\mu_0} \cdot \frac{V_{GS} - V_{TH,damaged}}{V_{GS} - V_{TH,pristine}}$$

This factor η represents the fractional current remaining after impact damage.

For split-channel devices, only the damaged splits contribute reduced current, while surviving splits maintain full performance, leading to:

$$\eta_{split} = \frac{1}{N_{splits}} \sum_{i=1}^{N_{splits}} eta_i$$

4.1.8 I-V Characteristics

For determining I-V characteristics, the linear and saturation region behavior is incorporated in the following equation to account for continuity between the regions.

$$I_D = I_{D,lin} \cdot f(\alpha) + I_{D,sat} \cdot (1 - f(\alpha))$$

$I_{D,lin}$ and $I_{D,sat}$ accounts for drain current in linear and saturation regions accordingly. f(α) is sigmoid function of, $\alpha = V_{DS} - V_{DS,sat}$

4.2 Impact scenario design and parametric study

4.2.1 Scenario Design

To simulate different impact stress, Tungsten ball radius (R) and drop height (H) was varied to simulate 6 different scenario.

Variation by height

- **Scenario 1:** R = 12 μm, H = 50 μm
- **Scenario 2:** R = 12 μm, H = 120 μm
- **Scenario 3:** R = 12 μm, H = 250 μm

Variation by radius

- **Scenario 4:** R = 10 μm, H = 120 μm
- **Scenario 5:** R = 20 μm, H = 120 μm
- **Scenario 6:** R = 30 μm, H = 120 μm

4.2.2 Architectural Comparison

Each impact scenario was simulated for three device configurations:

1. Conventional MOSFET (W = 3.2 μm)
2. Split-Channel MOSFET (5 splits, W_{eff} = 2 μm, W_{total} = 3.2 μm)
3. Split-Channel MOSFET - Equal Width (5 splits, W_{eff} = 3.2 μm, W_{total} = 4.4 μm)

Configuration 2 trade-offs effective channel width to introduce gap between splits. Configuration 3 increases device dimension to maintain equal effective channel width.

4.2.3 Performance Metrics

Primary Metrics:

- **Original Performance:** Drain current before impact stress at V_{GS} = 3.3 V
- **Performance Degradation (%):** Percentage reduction in drain current after impact compared to pristine device

Comparative Metric:

- **Improvement Factor (IF):** Ratio indicating how much better split-channel retains performance (reduces performance degradation) compared to conventional design under identical impact conditions

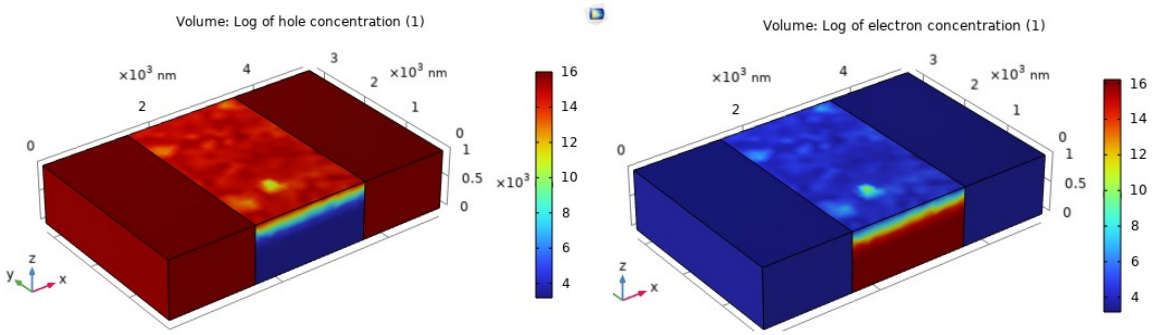
Damage Characterization:

- **Splits Affected:** Number of channel splits experiencing damage (split-channel only)

CHAPTER 5
RESULTS AND DISCUSSIONS

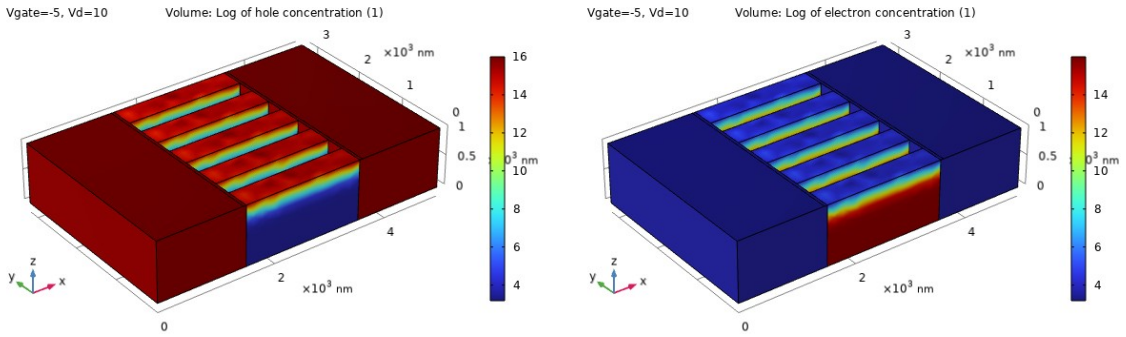
5.1 Results and Analysis

5.1.1 Carrier Distribution



Hole concentraton Electron concentraton

Fig. 5.1 Hole concentration and electron concentration in conventional MOSFET (PMOS)



Hole concentraton Electron concentraton

Fig. 5.2 Hole concentration and electron concentration in split channel MOSFET (PMOS)

Analysis: The carrier distribution simulations confirm that split-channel architecture maintains proper channel formation in each individual split. Air gaps provide electrical isolation, however, it does not compromise MOSFET functionality under normal operation.

5.1.2 Stress Distribution

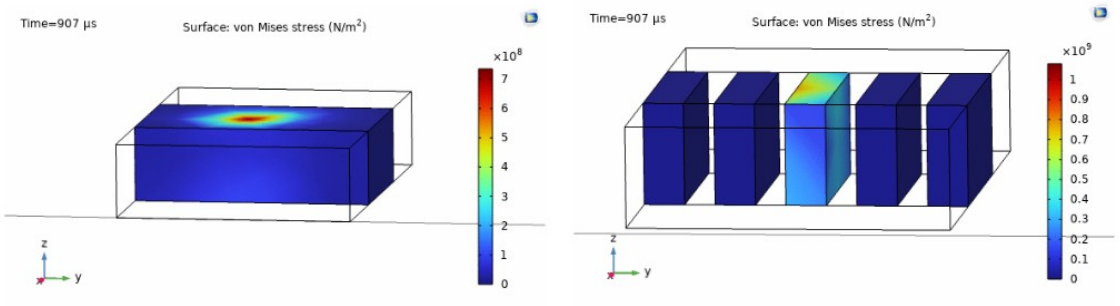


Fig. 5.3 Impact stress distribution in conventional MOSFET vs Split-Channel MOSFET

Analysis: Impact stress propagates throughout the entire channel in conventional MOSFETs, resulting in widespread device degradation. Split-channel MOSFETs confine stress to localized regions, with air gaps acting as mechanical barriers that prevent stress transmission to adjacent splits. This localized damage containment enables unaffected splits to maintain original performance.

5.1.3 I-V characteristics and performance comparison (at V_{GS} = 3.3 V)

5.1.3.1 Conventional vs Split Channel (W_{eff} = 2 µm, W_{total} = 3.2 µm)

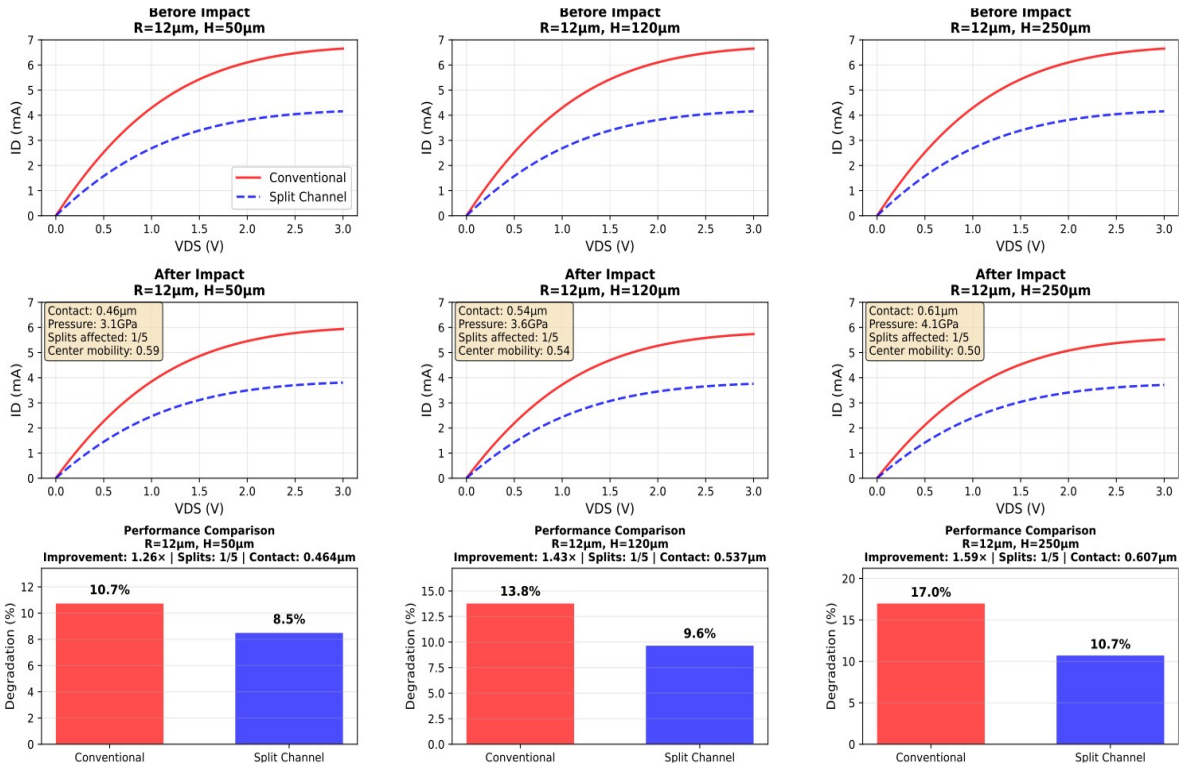


Fig. 5.4 I-V Characteristics and performance comparison for scenario 1-3 (W_{eff} = 2.0 µm)

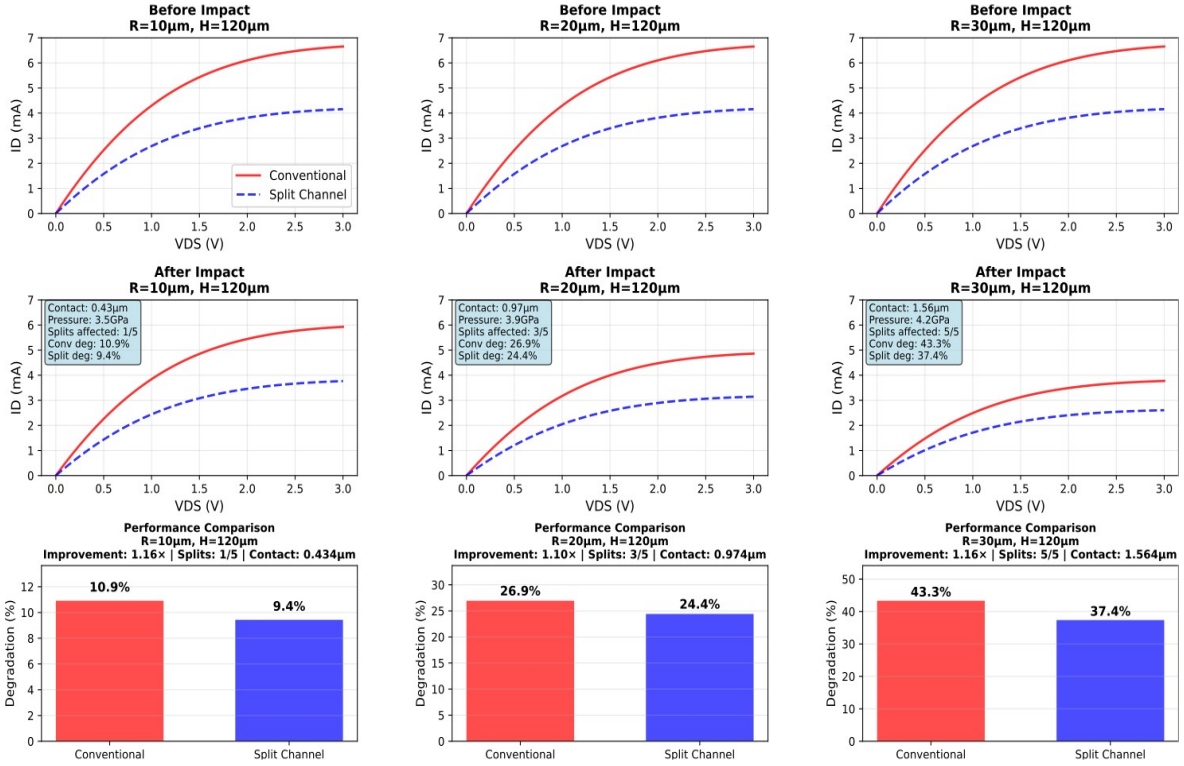


Fig. 5.5 I-V Characteristics and performance comparison for scenario 4-6 (W_{eff} = 2.0 µm)

Peformence metrics analysis:

- **Original performance:** Conventional MOSFET has higher drain current due to higher effective channel width
- **Performance Degradation:** After impact, split channel MOSFET shows less degradation in drain current compared to respective conventional device case
- **Improvement Factor (IF):** Depending on scenario, split channel architecture showed up to 1.59 times better performance retention
- **Splits Affected:** In most scenarios only one split is damaged. Multiple splits are damaged in two scenarios. In scenario 6, all 5 splits of split channel architecture went through damage. However, it still performed better, as damage severity has decreased due to air gap.

5.1.3.2 Conventional vs Split Channel – equal channel (W_{eff} = 3.2 µm, W_{total} = 4.4 µm)

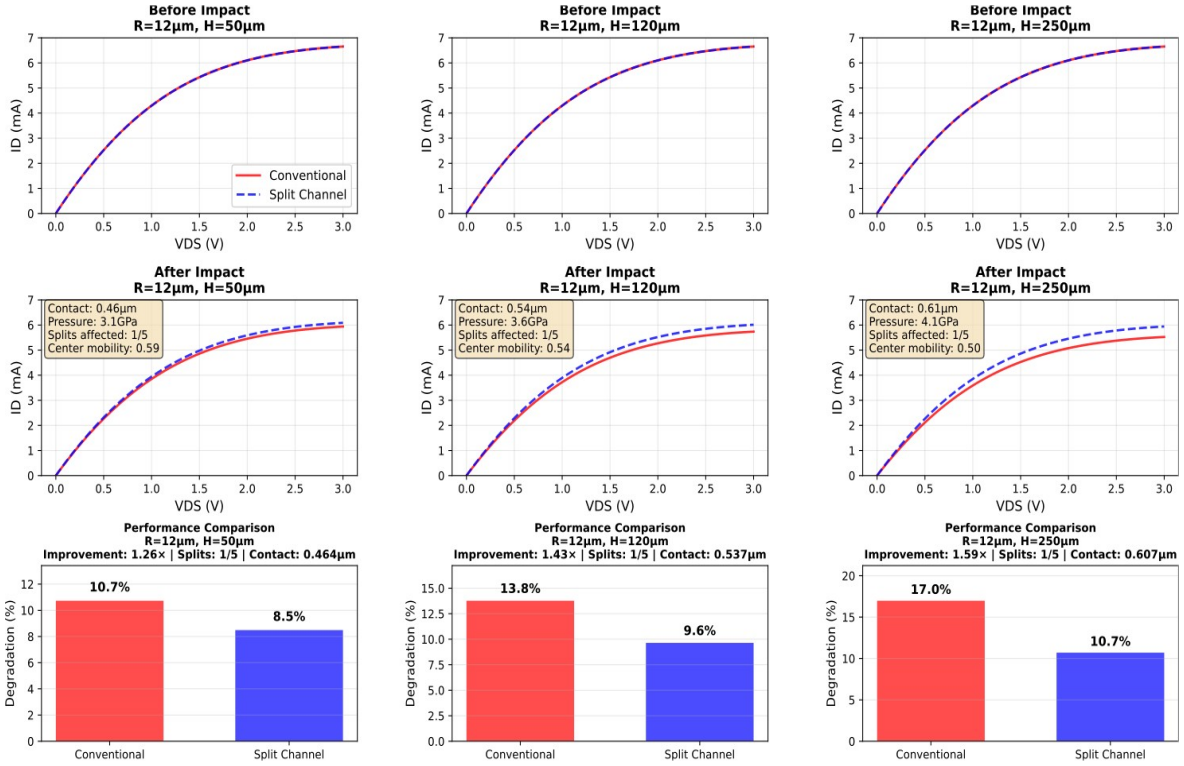
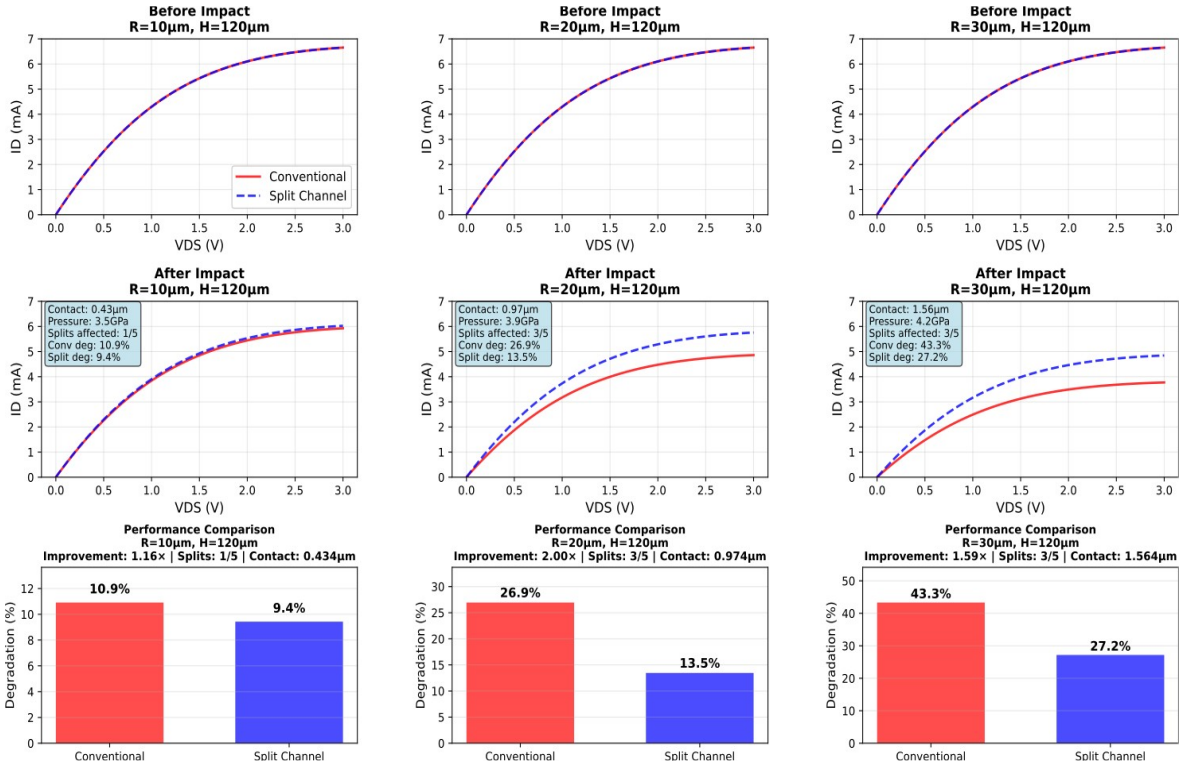


Fig. 5.6 I-V Characteristics and performance comparison for scenario 7-9 (W_{eff} = 3.2 µm)



5.7 I-V Characteristics and performance comparison for scenario 10-12 (W_{eff} = 3.2 µm)

Performance metrics analysis:

- **Original performance:** After accounting for equal effective channel width, both conventional and split channel MOSFETs exhibit equal original performance
- **Performance Degradation:** After impact, split channel MOSFET undergoes less performance degradation. In these cases, it actually results in outperforming conventional MOSFET after impact, as they had equal performance originally.
- **Improvement Factor (IF):** Depending on scenario, split channel architecture showed up to 1.59 times better performance retention
- **Splits Affected:** Up to 3 splits are damaged in split channel design in simulated scenarios.

5.2 Discussion

- Split channel design consistently shows to retain performance better after undergoing an impact stress. Conventional MOSFETs exhibit considerably higher performance degradation under impact stress. Split-channel designs maintain more reliable performance.
- The trade-off comes as decreased effective channel width for an equal outer dimension. However, in many applications, stable current is more important than higher current. Apart from that, the device can still be designed to achieve any arbitrary channel width.
- Some devices, such as sensors and wearables, are often exposed to environment and extreme conditions. In such scenarios, the device may be affected by dirt, insect contact, water drops, or accidental impacts during handling and usage. Split-channel architecture can prove to be a reliable solution in such cases.
- In other scenarios where probability of impact stress exposure is minimal, conventional MOSFET may still be preferred due to design simplicity and higher current density.

5.3 Limitations

- Computational resource constraints limited capability for finer-tuned simulation with higher mesh resolution and extensive parametric sweeps. Higher mesh density would improve stress field resolution but was infeasible within available computing infrastructure.

- Hardware prototype validation was not possible due to lack of fabrication facilities and equipment. Actually realizing the split channel design might come with critical challenges to overcome.
- Analysis focused on single-impact events; cumulative damage from repeated impacts (fatigue) and long-term reliability degradation were not investigated. Thermal effects during impact events and their influence on subsequent electrical characteristics were not taken into account.
- To understand the actual real-world scenario and applicability, the type and magnitude of impact stress that is likely, application-specific experiment and observation is required.

CHAPTER 6
DEMONSTRATION OF OUTCOME BASED EDUCATION (OBE)

6.1 Introduction

We conducted our work in alignment with Outcome-Based Education (OBE) principles, incorporating Course Outcomes (COs), Program Outcomes (POs), and Knowledge Profiles (K3-K8). This methodology allowed us to address real-world challenges in a feasible, sustainable, and ethical manner. Throughout the project, we navigated complex engineering problems, employing systematic problem-solving approaches while managing the multifaceted attributes of complex engineering activities.

6.2 Course Outcomes (COs) Addressed

The following table shows the COs addressed in the Thesis.

COs	CO Statement	POs	Put Tick (√)
CO1	Apply knowledge of electrical and electronic engineering to the solution of complex engineering problems.	PO1	√
CO2	Identify a contemporary real life problem related to electrical and electronic engineering by reviewing and analyzing existing research works.	PO2	√
CO3	Determine functional requirements of the problem considering feasibility and efficiency through analysis and synthesis of information.	PO4	√
CO4	Select a suitable solution and determine its method considering professional ethics, codes and standards.	PO8	√
CO5	Adopt modern engineering resources and tools for the solution of the problem.	PO5	√
CO6	Prepare management plan and budgetary implications for the solution of the problem.	PO11	
CO7	Analyze the impact of the proposed solution on health, safety, culture and society.	PO6	
CO8	Analyze the impact of the proposed solution on environment and sustainability.	PO7	√
CO9	Develop a viable solution considering health, safety, cultural, societal and environmental aspects.	PO3	
CO10	Work effectively as an individual and as a team member for the accomplishment of the solution.	PO9	√
CO11	Prepare various technical reports, design documentation, and	PO10	√

	deliver effective presentations for demonstration of the solution.		
CO12	Recognize the need for continuing education and participation in professional societies and meetings.	PO12	√

CO1: Apply knowledge of electrical and electronic engineering to the solution of complex engineering problems.

This project applies electrical and electronic engineering principles to address the impact of mechanical stress on semiconductor device performance and reliability in harsh operating conditions through MOSFET simulation and analysis.

CO2: Identify a contemporary real-life problem related to electrical and electronic engineering by reviewing and analyzing existing research works.

The problem addressed is the impact of mechanical stress on semiconductor device performance and reliability, which is critical in industries operating under harsh conditions.

CO3: Determine functional requirements of the problem considering feasibility and efficiency through analysis and synthesis of information.

Functional requirements include simulation of mechanical stress coupled with electrical properties analysis under stress conditions, and comparison of MOSFET designs using industry-standard tools.

CO4: Select a suitable solution and determine its method considering professional ethics, codes and standards.

The selected solution involves simulation software to model MOSFET behavior under mechanical stress, implemented in accordance with professional ethics and relevant standards.

CO5: Adopt modern engineering resources and tools for the solution of the problem.

COMSOL is utilized for simulation, and Python is employed for data analysis and visualization.

CO8: Analyze the impact of the proposed solution on environment and sustainability.

The proposed solution addresses environmental concerns by reducing e-waste and promoting long-lasting devices through stress-resilient design.

CO10: Work effectively as an individual and as a team member for the accomplishment of the solution.

The project demonstrates effective collaboration through clear roles and responsibilities, supported by regular progress meetings among team members.

CO11: Prepare various technical reports, design documentation, and deliver effective presentations for demonstration of the solution.

Technical reports, design documentation, and presentations have been prepared covering experimental setup, data collection methodology, and results analysis.

CO12: Recognize the need for continuing education and participation in professional societies and meetings.

The project acknowledges the importance of continued professional development through active participation in continuing education initiatives and engagement with professional societies to maintain current knowledge and meet evolving industry standards.

6.3 Aspects of Program Outcomes (POs) Addressed

The following table shows the aspects addressed for certain Program Outcomes (POs) addressed in the Thesis.

PO	Statement	Different Aspects	Put Tick (√)
PO3	**Design/development of solutions**: Design solutions for complex electrical and electronic engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.	Public health	
		Safety	√
		Cultural	
		Societal	
		Environmental	√
PO4	**Investigation:** Conduct investigations of complex electrical and electronic engineering problems using research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions.	Design of experiments	√
		Analysis and interpretation of data	√
		Synthesis of information	√
PO6	**The engineer and society:** Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to professional engineering practice and solutions to complex electrical and electronic engineering problems.	Societal	
		Health	
		Safety	√
		Legal	
		Cultural	
PO7	**Environment and sustainability:** Understand and evaluate the sustainability and impact of professional engineering work in the solution of complex electrical and electronic engineering problems in societal and environmental contexts.	Societal	
		Environmental	√
PO8	**Ethics:** Apply ethical principles embedded with	Religious values	

	religious values, professional ethics and responsibilities, and norms of electrical and electronic engineering practice.	Professional ethics and responsibilities	√
		Norms	
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	Comprehend and write effective reports	√
		Design documentation	√
		Make effective presentations	√
		Give and receive clear instructions	√
PO11	**Project management and finance:** Demonstrate knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	Engineering management principles	
		Economic decision-making	
		Manage projects	
		Multidisciplinary environments	√

6.4 Knowledge Profiles (K3 – K8) Addressed

The following table shows the Knowledge Profiles (K3 – K8) addressed in the Thesis.

K	Knowledge Profile (Attribute)	Put Tick (√)
K3	A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline	√
K4	Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline	
K5	Knowledge that supports engineering design in a practice area	√
K6	Knowledge of engineering practice (technology) in the practice areas in the engineering discipline	√
K7	Comprehension of the role of engineering in society and identified issues in engineering practice in the discipline: ethics and the engineer's professional responsibility to public safety; the impacts of engineering activity; economic, social, cultural, environmental and sustainability	√
K8	Engagement with selected knowledge in the research literature of the discipline	√

Explanation or justification of how the Knowledge Profiles (K3 – K8) will be addressed in the Thesis.

K	Explanation/Justification
K3	Formulation of the theory behind how mechanical stress impacts flexible electronics
K5	Design knowledge of flexible electronics
K6	Simulation techniques and methods
K7	Broader impacts will be considered
K8	Review of recent researches and finding research scopes

6.5 Use of Complex Engineering Problems

The project addresses several complex engineering problems that are critical for advancing the understanding and design of semiconductor devices under mechanical stress. One of the primary challenges is understanding how mechanical stress is distributed within semiconductor devices and how it affects their electrical properties. This involves conducting complex simulations and analyses to model stress-strain relationships and their impact on device performance. By accurately simulating these interactions, the project aims to provide insights into how mechanical stress influences the behavior of semiconductor devices.

Another key area of focus is investigating the reliability of MOSFETs with different channel architectures under various stress conditions. This includes analyzing failure modes, threshold voltage shifts, and mobility changes due to mechanical stress. Understanding these factors is essential for ensuring the long-term reliability and performance of semiconductor devices in applications where they are subjected to mechanical stress.

The project also involves designing and optimizing the geometry of split channel architectures to mitigate the effects of mechanical stress. This requires a deep understanding of both the mechanical and electrical properties of the materials involved. By optimizing the channel geometry, the project aims to enhance the robustness of semiconductor devices and improve their performance under stress.

Developing accurate and efficient simulation models is another critical aspect of the project. These models are used to predict the behavior of semiconductor devices under mechanical stress, balancing the need for detailed simulations with computational efficiency. This ensures that the simulations are both accurate and feasible to run, providing reliable predictions of device behavior.

6.6 Socio-Cultural, Environmental, and Ethical Impact

Socio-Cultural Impact

The project's technological advancements have significant socio-cultural implications. Enhanced reliability and durability of microelectronic systems can lead to more efficient and cost-effective solutions in industries like automotive, aerospace, telecommunications, and computing, positively impacting daily life. Additionally, more resilient semiconductor designs can enable innovations in wearable health monitors, flexible displays, and soft robotics, improving healthcare, entertainment, and industrial applications.

Ethical Impact

Environmentally, the semiconductor industry has a substantial footprint due to hazardous materials and high energy consumption. This project can promote sustainability by reducing electronic waste through longer-lasting devices and encouraging the use of environmentally friendly materials and fabrication processes.

Environmental Impact

Ethically, the project considers the potential misuse of advanced semiconductor technologies, such as surveillance or unauthorized data collection. It recognizes the importance of developing ethical guidelines to mitigate these risks and ensure data privacy and security. The project also emphasizes the need to consider the ethical use of resources, ensuring they are used responsibly and sustainably. Furthermore, efforts are directed toward making the benefits of these technologies accessible to all segments of society, promoting equitable access and improving lives across all socio-economic groups.

6.7 Attributes of Ranges of Complex Engineering Problem Solving (P1 – P7) Addressed

The following table shows the attributes of ranges of Complex Engineering Problem Solving (P1 – P7) addressed in the Thesis.

P	**Range of Complex Engineering Problem Solving**	**Put Tick (√)**
Attribute	Complex Engineering Problems have characteristic P1 and some or all of P2 to P7:	
Depth of knowledge required	**P1:** Cannot be resolved without in-depth engineering knowledge at the level of one or more of K3, K4, K5, K6 or K8 which allows a fundamentals-based, first principles analytical approach	√
Range of conflicting requirements	**P2:** Involve wide-ranging or conflicting technical, engineering and other issues	√
Depth of analysis required	**P3:** Have no obvious solution and require abstract thinking, originality in analysis to formulate suitable models	√

Familiarity of issues	**P4:** Involve infrequently encountered issues	
Extent of applicable codes	**P5:** Are outside problems encompassed by standards and codes of practice for professional engineering	
Extent of stakeholder involvement and conflicting requirements	**P6:** Involve diverse groups of stakeholders with widely varying needs	√
Interdependence	**P7:** Are high level problems including many component parts or sub-problems	

Explanation or justification of how the attributes of ranges of Complex Engineering Problem Solving (P1 – P7) will be addressed in EEE 4700 (Project and Thesis).

P	Explanation/Justification
P1	Up to date knowledge and tools will be required
P2	Several contflicting issues has to be balanced in design
P3	Different designs may provide advantage in different specifics, with different trade-offs
P6	Electronic devices are widely used by diverse groups

6.8 Attributes of Ranges of Complex Engineering Activities (A1 –A5) Addressed

The following table shows the attributes of ranges of Complex Engineering Activities (A1 – A5) addressed in the Thesis.

A	Range of Complex Engineering Activities	Put Tick (√)
Attribute	Complex activities means (engineering) activities or projects that have some or all of the following characteristics:	
Range of resources	**A1:** Involve the use of diverse resources (and for this purpose resources include people, money, equipment, materials, information and technologies)	√
Level of interaction	**A2:** Require resolution of significant problems arising from interactions between wide-ranging or conflicting technical, engineering or other issues	√
Innovation	**A3:** Involve creative use of engineering principles and research-based knowledge in novel ways	√
Consequences for society and the environment	**A4:** Have significant consequences in a range of contexts, characterized by difficulty of prediction and mitigation	
Familiarity	**A5:** Can extend beyond previous experiences by applying principles-based approaches	√

Explanation or justification of how the attributes of ranges of Complex Engineering Activities (A1 – A5) have been addressed in the Thesis.

A	Explanation/Justification
A1	Involvement of study and research materials, expert supervision, up to date

	knowledge and technology
A2	Significant problems may arise from conflicting requirements, such as ensuring both mechanical flexibility and electrical performance.
A3	Engineering principles and research is applied to develop more flexible electronic devices.
A5	The project extends beyond previous experiences by applying and adapting existing engineering principles to new challenges in flexibleMarket adoption would depend on manufacturing scalability, cost-effectiveness, and industry acceptance of the novel architecture. electronics.

CHAPTER 7
CONCLUSION

7.1 Summary of Research Objectives and Findings

7.1.1 Research Problem and Approach

- Recap the fundamental gap: insufficient understanding of how localized impact mechanical stress degrades MOSFET electrical characteristics
- Highlight the absence of architectural solutions specifically designed for impact resilience (as distinct from continuous stress mitigation)
- Briefly describe the three-stage methodology: device design → impact stress simulation → electrical performance prediction

7.1.2 Primary Findings

- **Conventional MOSFET behavior**: Impact stress propagates uniformly across entire channel; widespread degradation with no damage containment
- **Split-channel performance**: Air gaps confine stress to localized regions; performance degradation reduced by up to 1.59× (Improvement Factor)
- **Impact scenario dependence**: Protection effectiveness depends on ratio of impact radius to sub-channel width—maximum benefit for localized impacts, diminished for distributed impacts
- **Trade-offs**: Effective channel width reduced by 37.5% for same outer dimensions; equal-width configurations increase outer dimensions to 4.4 μm

7.2 Physical Mechanisms Underlying Protection

7.2.1 Acoustic Impedance Mismatch

- Silicon acoustic impedance: ~20 MPa·s/m vs. air: ~400 Pa·s/m (~50,000:1 ratio)
- Reflection coefficient at silicon-air interfaces: $R \approx 0.999$
- Result: Approximately 99.9% of stress wave energy reflects at each air gap, preventing transmission to adjacent splits

7.2.2 Stress Wave Attenuation and Graceful Degradation

- Exponential decay of stress field with distance from impact point

- Stress magnitude in non-impacted splits attenuated by factor of R^n (where n = number of gaps)
- Performance degrades proportionally with damaged splits (e.g., one of five splits failed = 80% retained performance)
- Contrast: Conventional devices suffer catastrophic degradation from single damage point

7.3 Key Contributions to the Field

7.3.1 Novel Architectural Approach

- First comprehensive analysis of split-channel MOSFETs specifically for impact mechanical stress in CMOS devices
- Extends prior work (Urmi et al., 2022) from display applications with large polycrystalline TFTs to conventional MOSFET technology

7.3.2 Integrated Simulation Framework

- Coupled mechanical-electrical modeling enables prediction of device performance degradation from specified impact conditions
- Fills critical gap in existing tools that address only mechanical or electrical domains separately
- Methodology generalizable to other semiconductor device types

7.3.3 Quantitative Design Guidelines

- Systematic parametric analysis (6 scenarios) establishes when split-channel protection provides meaningful benefits
- Performance metrics (degradation factors, improvement ratios, damage isolation effectiveness) enable informed architecture selection
- Decision framework: high-impact-exposure applications benefit from split-channel design; protected applications may prefer conventional architecture

7.4 Application Domains and Practical Impact

7.4.1 Target Applications

- **Wearable and portable electronics**: Health monitors, fitness trackers, smartwatches face repeated mechanical shocks; split-channel enables durability without bulky protective casings
- **Environmental sensing systems**: IoT nodes in agricultural, industrial, and remote monitoring applications routinely exposed to impact; enhanced resilience reduces maintenance costs
- **Flexible and stretchable electronics**: Emerging applications in conformable sensors, electronic skin, biomedical implants benefit from combined mechanical flexibility and impact resilience
- **Manufacturing and supply chain**: Impact events during assembly, testing, and handling contribute to yield loss; understanding damage mechanisms informs better handling procedures

7.4.2 Broader Context

The transition from protected laboratory environments to ubiquitous real-world deployment demands that mechanical reliability receive attention equal to electrical performance. As semiconductor devices miniaturize and proliferate into diverse environments, mechanical resilience becomes increasingly critical.

7.5 Limitations and Scope Constraints

7.5.1 Computational and Fabrication Limitations

- Mesh resolution constrained by available computing infrastructure
- Hardware prototype validation not feasible within project scope
- Actual fabrication may introduce manufacturing challenges not captured in simulation

7.5.2 Physical Scope Limitations

- Analysis focused on single impact events; cumulative fatigue damage not investigated
- Thermal transients during impact not considered (isothermal analysis at 300 K)

- Analysis limited to relatively large device dimensions (2 μm channel length); applicability to advanced CMOS nodes (<100 nm) requires further investigation

7.5.3 Model Validation

- Physics-based validation performed; experimental validation not feasible within project timeline
- Material properties sourced from literature; device-specific variations not characterized

7.6 Recommendations for Future Work

7.6.1 Experimental Validation

- Fabricate prototype split-channel MOSFETs in thin-film technology
- Conduct drop-test and mechanical impact experiments to validate simulation predictions
- Characterize actual I-V degradation under controlled impact scenarios

7.6.2 Extended Simulation Studies

- Incorporate cumulative damage from repeated impact events
- Analyze thermal transients and temperature effects during impact
- Extend analysis to advanced CMOS nodes and compound semiconductors (GaAs, GaN)

7.6.3 Design Optimization

- Optimize number, width, and gap spacing of splits for specific application scenarios
- Explore alternative gap materials (silicon dioxide, silicon nitride) versus air
- Investigate hierarchical multi-level channel segmentation

7.6.4 Circuit and System Integration

- Develop circuit design techniques exploiting split-channel redundancy (dynamic reconfiguration, fault tolerance)
- Explore co-design of split-channel devices with mechanical shock absorbers and protective packaging
- Characterize real-world impact scenarios in specific applications to develop context-dependent design guidelines

7.7 Concluding Remarks

Split-channel MOSFET architecture offers a practical solution for applications requiring improved mechanical resilience without sacrificing fundamental device functionality. The acoustic impedance mismatch at air gaps provides reliable stress isolation under localized impact conditions, enabling graceful degradation rather than catastrophic failure.

The design strategies and physical insights from this research provide a foundation for creating robust, field-deployable semiconductor systems capable of withstanding real-world mechanical challenges while maintaining the performance and efficiency required by modern applications. This work establishes that architectural innovation at the device level can meaningfully enhance mechanical resilience through fundamental understanding of impact damage physics.

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Appendix A

A.1 Material properties

Silicon (MOSFET Substrate and Channel):

- Young's modulus: E_{Si} = 130 GPa
- Poisson's ratio: ν_{Si} = 0.28
- Density: ρ_{Si} = 2329 kg/m³
- Yield strength: σ_y = 7 GPa
- Longitudinal wave velocity: c_L = 8433 m/s
- Transverse wave velocity: c_T = 5843 m/s
- Acoustic impedance: $Z_{Si} \approx$ 20 MPa·s/m

Tungsten (Impact Ball):

- Young's modulus: E_W = 411 GPa
- Poisson's ratio: ν_W = 0.28
- Density: ρ_W = 19250 kg/m³

Air (Gap Medium in Split-Channel Design):

- Density: ρ_{air} = 1.2 kg/m³
- Acoustic impedance: $Z_{air} \approx$ 400 Pa·s/m

Electron Transport Properties:

- Pristine electron mobility: μ_0 = 1350 cm²/V·s (at 300 K)

A.2 Characteristics velocity

$$v_{char} = \sqrt{\frac{F_{static}}{m_w \cdot E_{eff} / R}}$$

where, F_{static} accounts for force due to weight = mg

A.3 Reflection coefficient

$$R = \left(\frac{Z_{air} + Z_{Si}}{Z_{air} - Z_{Si}} \right) \approx -0.999$$

A.4 MOSFET I-V Characteristics

In linear region,

$$I_{D,lin} = \mu_{eff} C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

In saturation region

$$I_{D,sat} = \frac{\mu_{eff} C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2$$

A.5 Sigmoid Function

$$f(\alpha) = \frac{1}{1 + e^{\alpha}}$$